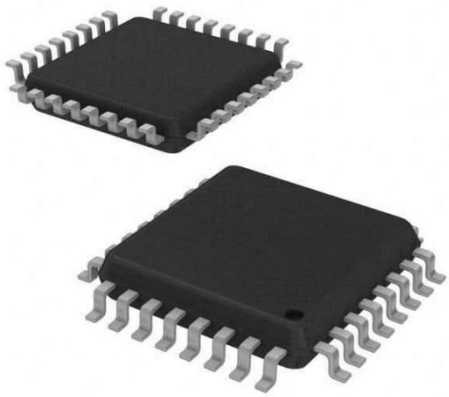
Description

The US5D1510 is a 2-GHz,10-output differential high-performance clock fanout buffer.

The US5D1510 is a low skew, high performance 1-to-10 clock fanout buffer. The US5D1510 clock buffer distributes one clock input to 10 pairs of differential LVDS clock outputs with minimum skew for clock distribution. The inputs can either be LVDS,LVPECL, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 2.5V/3.3V core power supply, and either a 2.5V/3.3V output operating supply.



Features

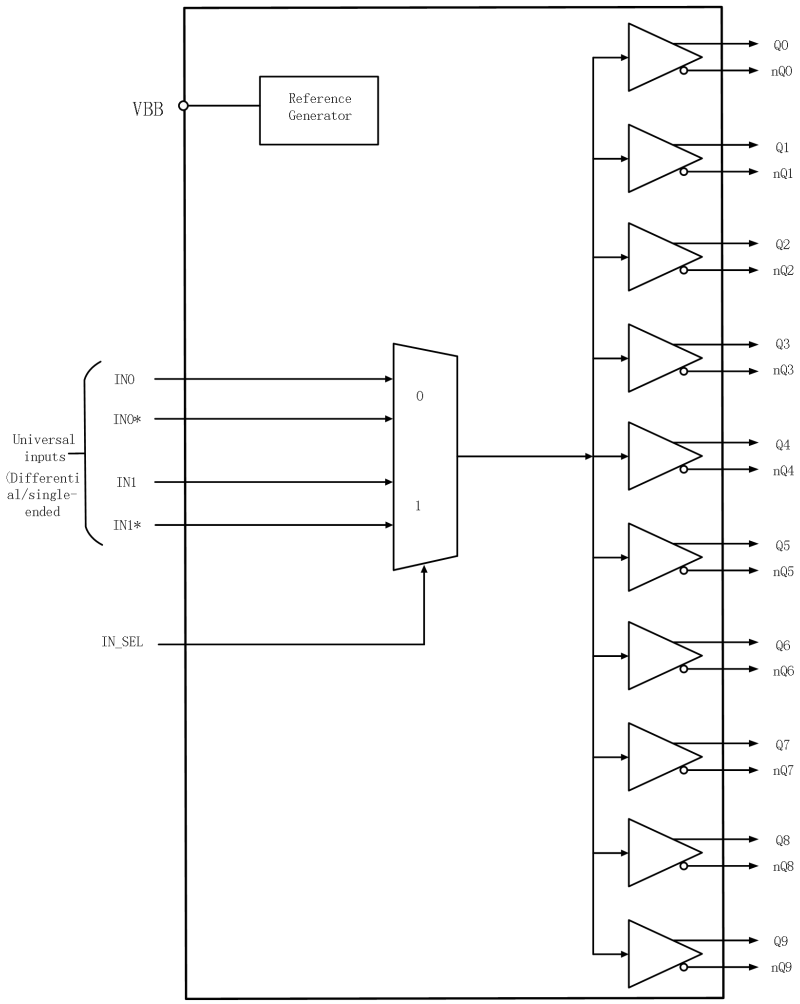
- 1:10 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS，HCSL and LVCMOS
- Ten LVDS outputs
- Maximum Output Frequency LVDS: 2-GHz
- Maximum Propagation Delay: 0.5ns(typical)
- Output skew: 30 ps (Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz: TBD fs RMS （12kHz - 20MHz)
- Supply voltage mode VDD: 2.5V±5%,3.3V±5%
- Industrial Temperature Range:-40°C to 85°C
- Available in QFP-32(7mm x 7mm) package

Applications

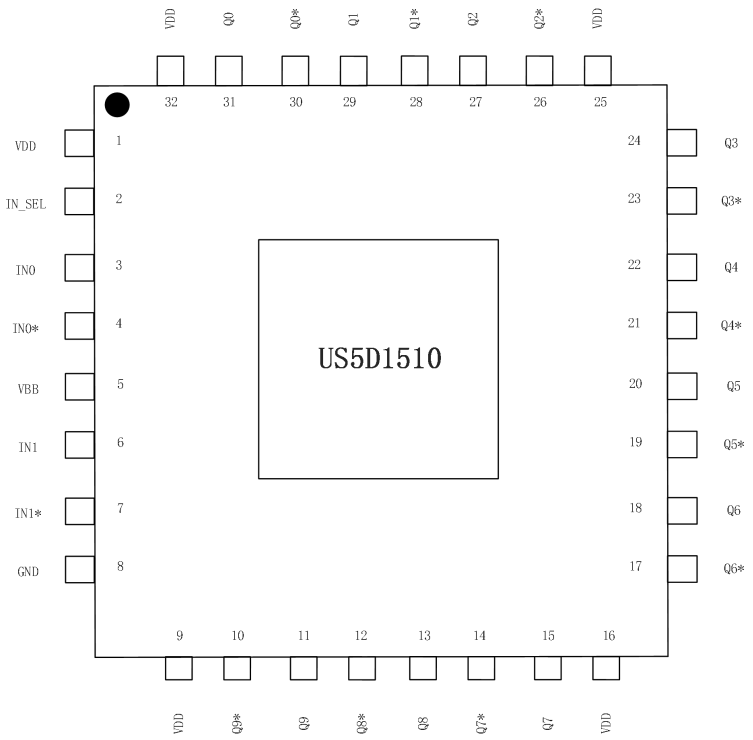
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

E-mail : sales@ultrasilicon.com.cn

Block Diagram



Pin Assignment for QFP-32 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	VDD	Power	Power supply for Core, 3.3V or 2.5V.
2	CLK_SEL	Input	Input selection with an internal 150-kΩ pulldown, selects input port.
3	IN0	Input	Differential input pair .
4	IN0*	Input	Differential input pair or single ended input.
5	VBB	Output	LVDS reference voltage output.
6	IN1	Input	Differential input pair .
7	IN1*	Input	Differential input pair or single ended input.
8	GND	Power	Ground.
9	VDD	Power	Power supply for Core, 3.3V or 2.5V.
10	Q9*	Output	Differential LVDS output pair.
11	Q9	Output	Differential LVDS output pair.
12	Q8*	Output	Differential LVDS output pair.
13	Q8	Output	Differential LVDS output pair.
14	Q7*	Output	Differential LVDS output pair.
15	Q7	Output	Differential LVDS output pair.
16	VDD	Power	Power supply for Core, 3.3V or 2.5V.
17	Q6*	Output	Differential LVDS output pair.
18	Q6	Output	Differential LVDS output pair.
19	Q5*	Output	Differential LVDS output pair.
20	Q5	Output	Differential LVDS output pair.
21	Q4*	Output	Differential LVDS output pair.
22	Q4	Output	Differential LVDS output pair.
23	Q3*	Output	Differential LVDS output pair.
24	Q3	Output	Differential LVDS output pair.
25	VDD	Power	Power supply for Core, 3.3V or 2.5V.
26	Q2*	Output	Differential LVDS output pair.
27	Q2	Output	Differential LVDS output pair.
28	Q1*	Output	Differential LVDS output pair.
29	Q1	Output	Differential LVDS output pair.
30	Q0*	Output	Differential LVDS output pair.
31	Q0	Output	Differential LVDS output pair.
32	VDD	Power	Power supply for Core, 3.3V or 2.5V.

Table 2: Input Selection Table

CLK_SEL	CLOCK INPUT
0	IN0,IN0*
1	IN1,IN1*

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	2.5-5% 3.3-5%	2.5 3.3	2.5+5% 3.3+5%	V

Electrical Characteristics

VDD = 3.135 V to 3.6 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
IDD	Power supply current	VDD=3.3V, F_{IN}=156.25MHz, All outputs active	-	210	-	mA
		VDD=2.5V, F_{IN}=156.25MHz, All outputs active	-	200	-	mA
LVCMOS INPUT						
F_{IN}	Input frequency	VDD=3.3V	0.1		250	MHz
Vth	input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
VIH	Input high voltage		0.7*VDD		VDD	V
VIL	Input low voltage		0		0.3*VDD	V

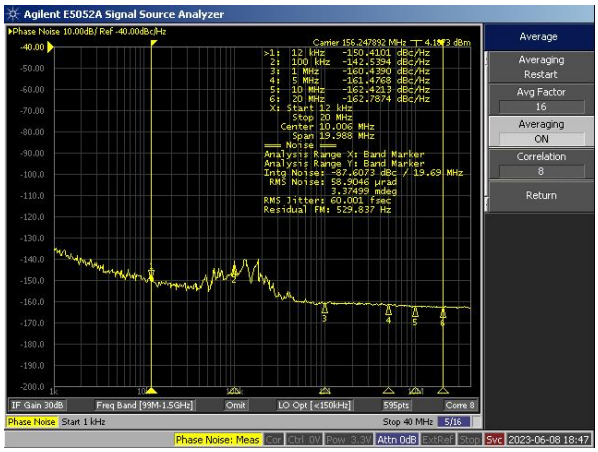
Electrical Characteristics(Continued)

VDD = 3.135 V to 3.6 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT						
F_{IN}	Input frequency	VDD=3.3V	0.1		2000	MHz
V_{IH1}	Input high voltage, LVDS input clocks				VDD+0.3	V
V_{IL1}	Input low voltage, LVDS input clocks		-0.3			V
V_{ICM}	Input common mode voltage		0.5		VDD-0.2	V
I_{IH}	Input high current	Input=VDD[1]			150	μA
I_{IL}	Input low current	Input=GND[1]	-150			μA
C_{IN}	Input capacitance	Measured ar 10MHz per pin			3	pF
LVDS OUTPUT						
VOD	Differential output voltage magnitude		250		450	mV
ΔVOD	Change in differential output voltage magnitude		-15		15	mV
VOC(ss)	Steady-state common mode output voltage		1.1		1.375	V
ΔVOC(ss)	Steady-state common mode output voltage		-15		15	mV
t_{PD}	Propagation delay	3.3V@156.25MHz		0.5	1.5	ns
$t_{SK,pp}$	Part-to-part skew				600	ps
$t_{SK,O}$	Output skew			10	30	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input,crossingpoint-to-crossing-point distortion	-50		50	ps
t_{RJIT}	Random additive jitter	50% duty cycle input, 12 kHz to 20 MHz,VDD=3.3V@156.25MHz		TBD	---	fs
t_R/t_F	Output rise time,tR	20% to 80%		160	300	ps
	Output fall time,tF	20% to 80%		160	300	ps
VBB	Reference output voltage	0 to 150uA output current，VDD=2.5V	1.125		1.375	V

(1).Positive current flows into the input pin, negative current flows out of the input pin.

PHASE JITTER



(a)Jitter_Source **(b)3V3_156M25_LVDS**

Figure 1 .RMS_Jitter_3V3=Sqrt(87^2-60^2)=64fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

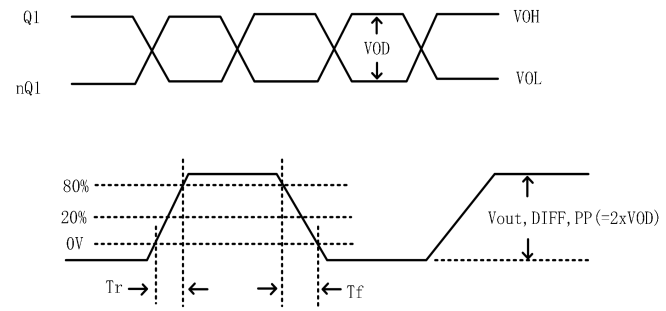
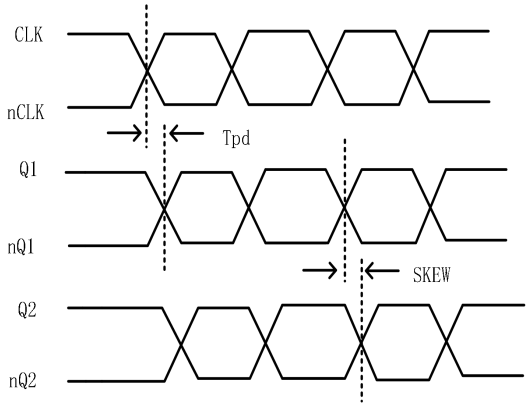


Figure 2.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 3.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

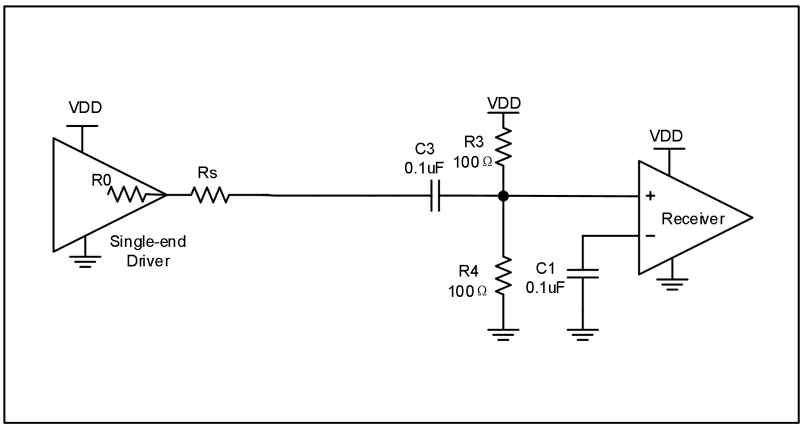
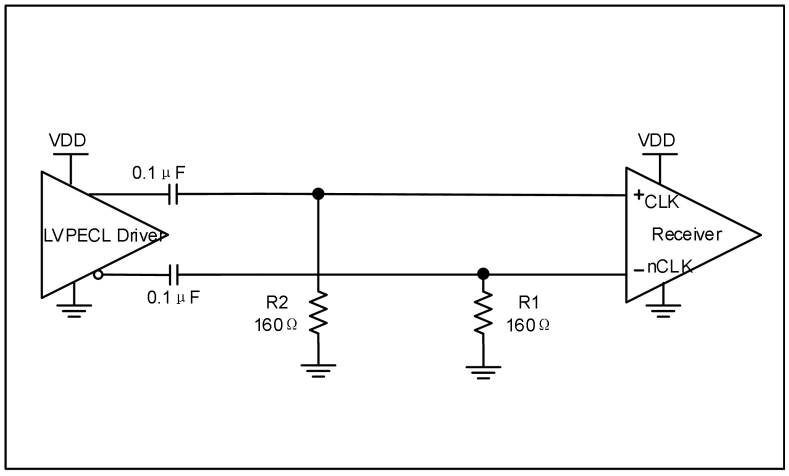
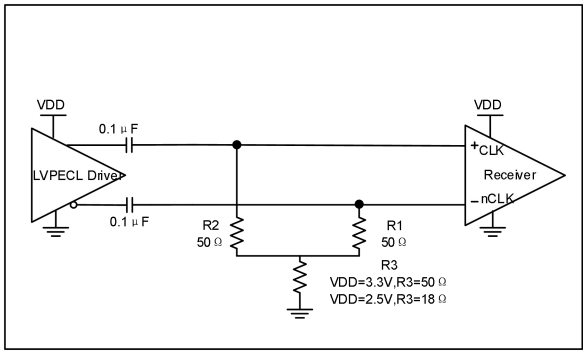


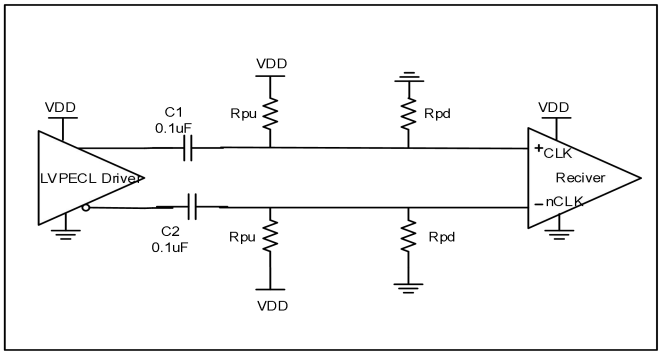
Figure4.Single-ended input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure8 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

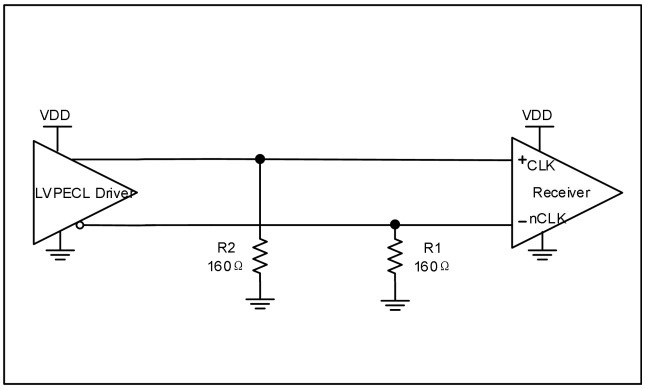


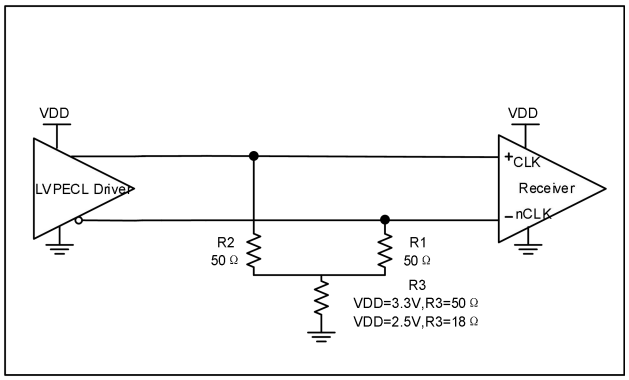


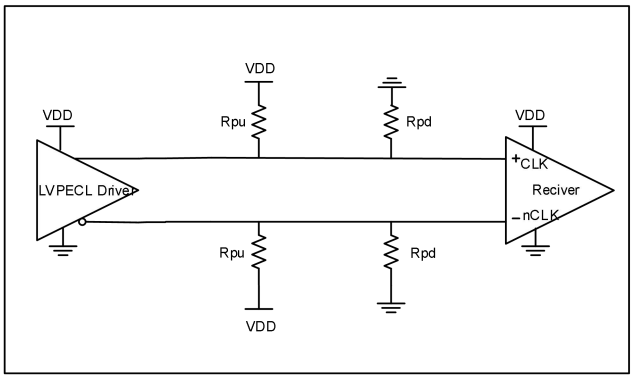


VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure5.LVPECL Driver(AC)

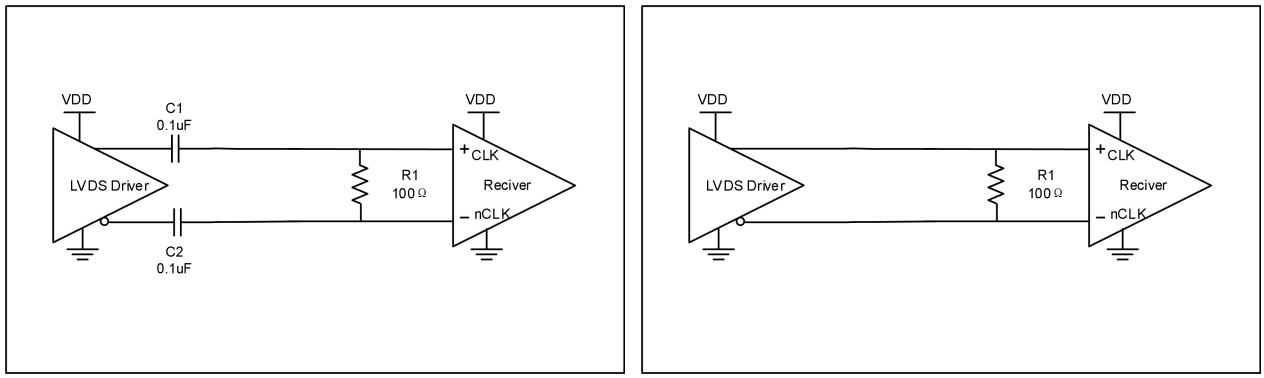






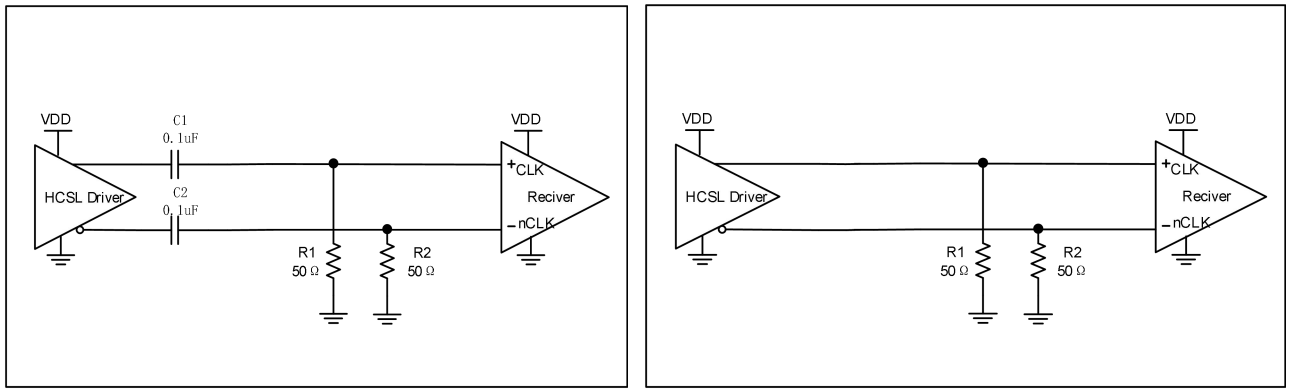
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure6.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

Figure7.LVDS Driver



a)AC coupling **b)DC coupling**

Figure8.HCSL Driver

Output connection circuit

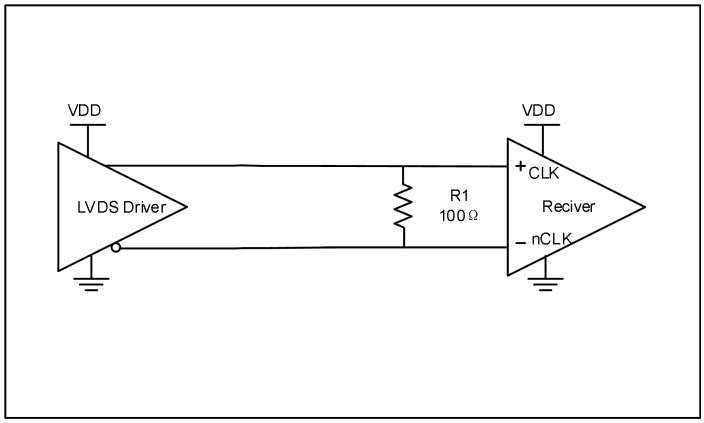
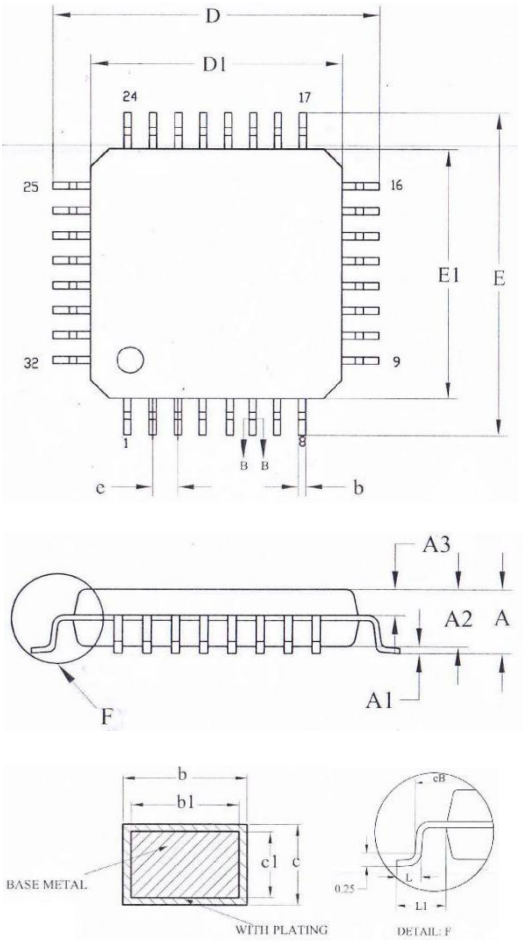


Figure9.LVDS Driver

PACKAGE DIMENSIONS(QFP-32)



符号	单位：mm		
	最小值	典型值	最大值
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	---	0.41
b1	0.32	0.35	0.38
c	0.13	---	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	---	8.25
e	0.80BSC		
L	0.45	---	0.75
L1	1.00REF		
θ	0°	---	7°

Reflow profile

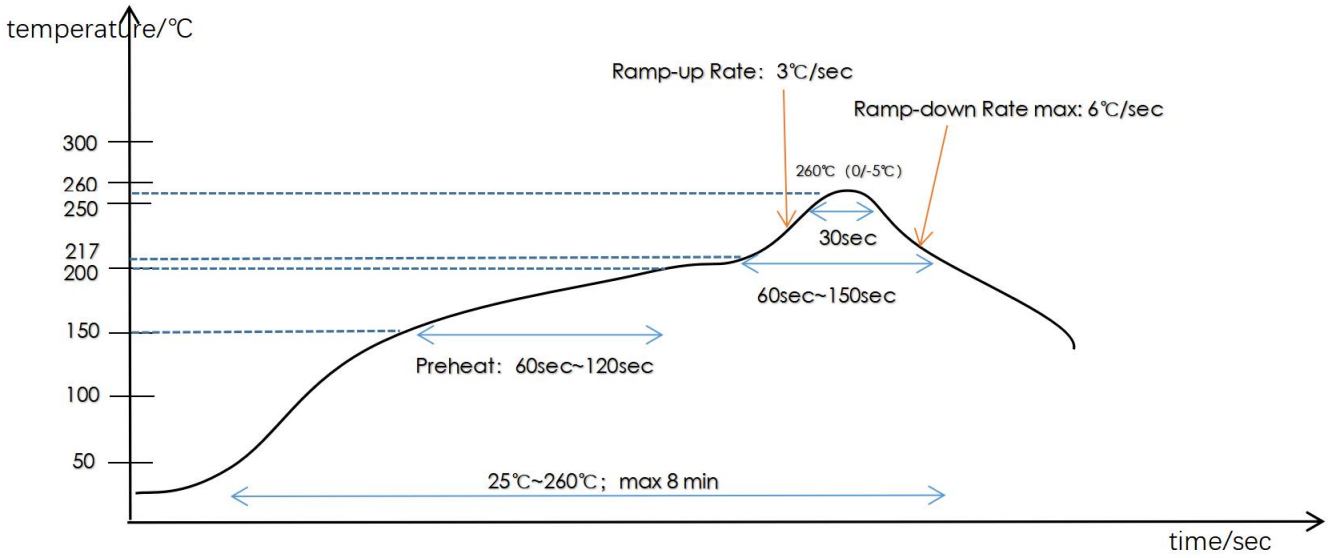


Figure10: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.11.27	First Draft.	1.0
2023.12.07	Edit Package dimensions.	1.5
2024.04.23	Modify electrical parameters.	2.0