# Description

The US5D102M is a 2-GHz,2-output differential high-performance clock fanout buffer.

The input clock is a differential input. The selected input clock is distributed to a LVPECL differential output.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

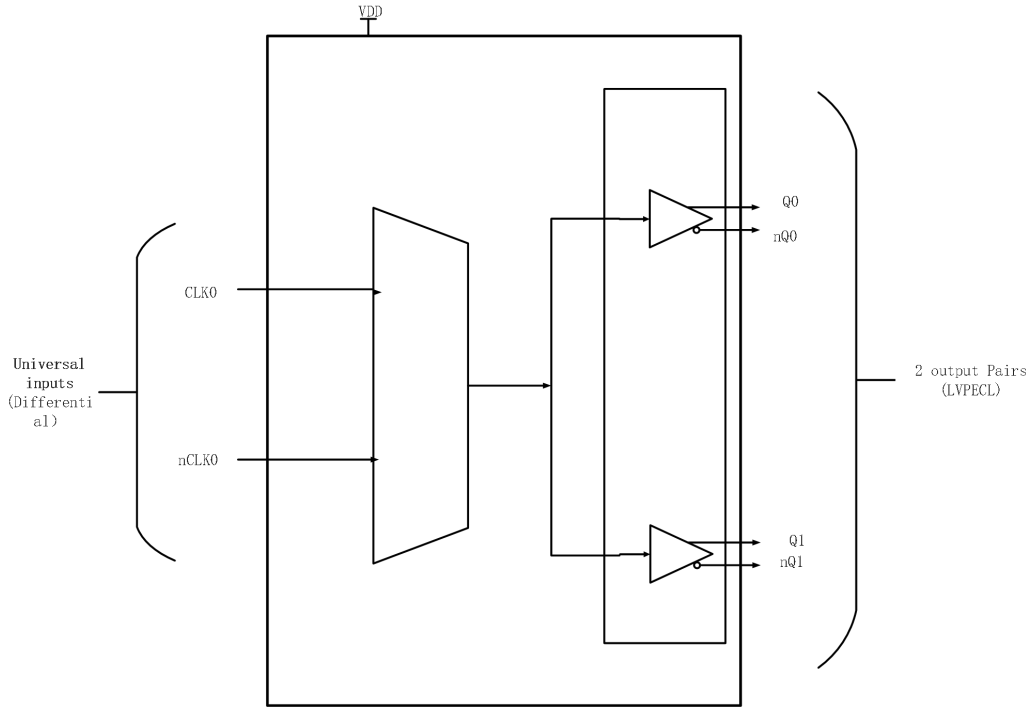
# Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

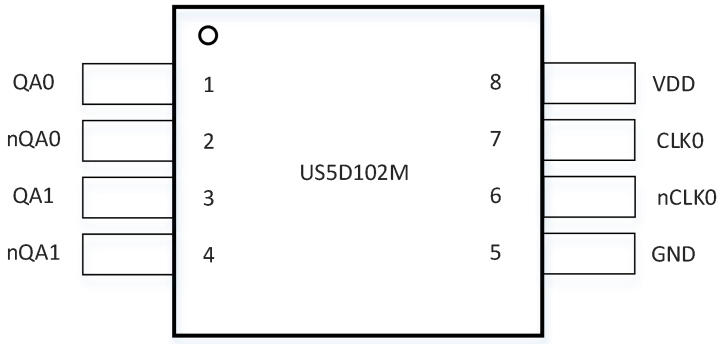
# Features

- A differential clock input pairs
- Maximum Output Frequency LVPECL - 2GHz
- Two differential output pairs that can be configured as LVPECL
- Output skew: 20ps (typical)
- Part-to-part skew: 300ps (Maximum)
- Additive RMS phase jitter @ 156.25MHz: 80fs RMS (12kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage mode: VDD=3.3Vor2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in 8-pin MSOP package

## Block Diagram




**Pin Assignment for 8-pin TSSOP Package**



# Pin Description and Pin Characteristic Tables

**Table 1: Pin Descriptions**[1]

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | QA0 | Output | Differential clock output pair. LVPECL |
| 2 | nQA0 | Output | Differential clock output pair. LVPECL |
| 3 | QA1 | Output | Differential clock output pair. LVPECL |
| 4 | nQA1 | Output | Differential clock output pair. LVPECL. |
| 5 | GND | Power | Ground. |
| 6 | nCLK0 | Input | Inverting differential clock. Internally biased to $0.5V_{DD}$. |
| 7 | CLK0 | Input | Non-inverting differential clock. Internally biased to ground. |
| 8 | $V_{DD}$ | Power | Power supply for Core and input Buffer blocks, 3.3V or 2.5V. |

# Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

| Item | Rating |
|---|---|
| $V_{DD}$ | 4.6V |
| $V_{IN}$ | -0.3V to $V_{DD}$ + 0.3V |
| $T_J$ :Junction Temperature | 150°C |
| $T_{STG}$ :Storage Temperature | -65°C to 150°C |

# ESD Ratings

| | | Max | Unit |
|---|---|---|---|
| V(ESD) Electrostatic discharge | Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017 | ±2500 | V |
| | Machine model (MM), JEDEC Std. JESD22-A115-C | ±250 | |
| | Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018 | ±750 | |

# Latch up

| | | Max | Unit |
|---|---|---|---|
| Latch up | I-test, JEDEC STD JESD78E | ±200 | mA |
| | V-test, JEDEC STD JESD78E | 4.6 | V |

## Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient air temperature | -40 | | 85 | °C |
| $T_J$ | Junction temperature | | | 125 | °C |
| $V_{DD}$ | Power supply for Core and input Buffer blocks | 3.3-5%<br>2.5-5% | 3.3<br>2.5 | 3.3+5%<br>2.5+5% | V |

## Electrical Characteristics

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns.
and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Universal Clock Inputs (CLK0/nCLK0, CLK1/nCLK1)** | | | | | | |
| $f_{CLKin}$ | Input Frequency Range(4) | Functional up to 2-GHz | 0.1 | | 2000 | MHz |
| $V_{IHD}$ | Differential Input High Voltage | CLKin driven differentially | | | VDD | V |
| $V_{ILD}$ | Differential Input Low Voltage | | GND | | | V |
| $V_{ID}$ | Differential Input Voltage Swing (5) | | 0.15 | | 1.3 | V |
| $V_{CMD}$ | Differential Input Common Mode Voltage | $V_{ID}$ = 150 mV | 0.25 | | VDD - 1.2 | V |
| | | $V_{ID}$ = 350 mV | 0.25 | | VDD - 1.1 | |
| | | $V_{ID}$ = 800 mV | 0.25 | | VDD - 0.9 | |
| $V_{IH}$ | Single-Ended Input High Voltage | CLK_X driven single-ended (AC or DC coupled), nCLK_X AC coupled to GND or externally biased within $V_{CM}$ range | | | VDD | V |
| $V_{IL}$ | Single-Ended Input Low Voltage | | GND | | | V |
| $V_{I\_SE}$ | Single-Ended Input Voltage Swing (6)(7) | | 0.3 | | 2 | Vpp |
| $V_{CM}$ | Single-Ended Input Common Mode Voltage | | 0.25 | | VDD - 1.2 | V |
| IEE | Working current | $F_{IN}$=156.25MHz,VDD=3.3V | | 90 | | mA |
| | | $F_{IN}$=156.25MHz,VDD=2.5V | | 70 | | |

(1) Specification is ensured by characterization and is not tested in production.
(2) See $V_{ID}$ =Differential input Voltage Swing, $V_{OD}$ = Differential output Voltage Swing.
(3) Parameter is specified by design, not tested in production.
(4) For clock input frequency ≥ 100 MHz, CLK_X can be driven with single-ended (LVCMOS) input swing up to 3.3 Vpp. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 Vpp max to prevent input saturation.

# Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns.
and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LVPECL Outputs** | | | | | | |
| $f_{CLKout}$ | Maximum Output Frequency | VDD=3.3V,$R_T$ = 160 Ω to GND | 0.1 | | 2000 | MHz |
| $Jitter_{ADD}$ | Additive RMS Jitter | CLKin: 156.25 MHz (12kHz-20MHz) | | 80 | 120 | fs |
| DUTY | Duty Cycle(4) | 50% input clock duty cycle | 45% | | 55% | |
| $V_{OH}$ | Output High Voltage | $T_A$ = 25 °C, DC Measurement, $R_T$ = 50 Ω toVDDO - 2 V | VDDO - 1.2 | VDDO - 0.99 | VDDO - 0.7 | V |
| $V_{OL}$ | Output Low Voltage | | VDDO - 2.0 | VDDO - 1.75 | VDDO - 1.5 | V |
| $V_{OD}$ | Output Voltage Swing (5) | | 600 | 760 | 1000 | mV |
| $t_R$ | Output Rise Time 20% to 80%(6) | $R_T$ = 160 Ω to GND, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, $R_L$ = 100 Ω differential, $C_L$ ≤ 5 pF | | 120 | 500 | ps |
| $t_F$ | Output Fall Time 80% to 20%(6) | | | 120 | 500 | ps |

(5) See *Typical Characteristics* for output operation over frequency.
(6) For the156.25 MHz clock input conditions, Additive RMS Jitter ($J_{ADD}$) is calculated using Method : $J_{ADD}$ = SQRT($J_{OUT}^2$ - $J_{SOURCE}^2$), where $J_{OUT}$ is the total RMS jitter measured at the output driver and $J_{SOURCE}$ is the RMS jitter of the clock source applied to CLKin.
(7) 156.25 MHz LVDS input clock source from Epson SG3225VEN(LVDS) Low-Noise SPXO.
(8) 156.25 MHz LVPECL input clock source from Epson SG3225VEN(LVPECL) Low-Noise SPXO.
(9) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz.
(10) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

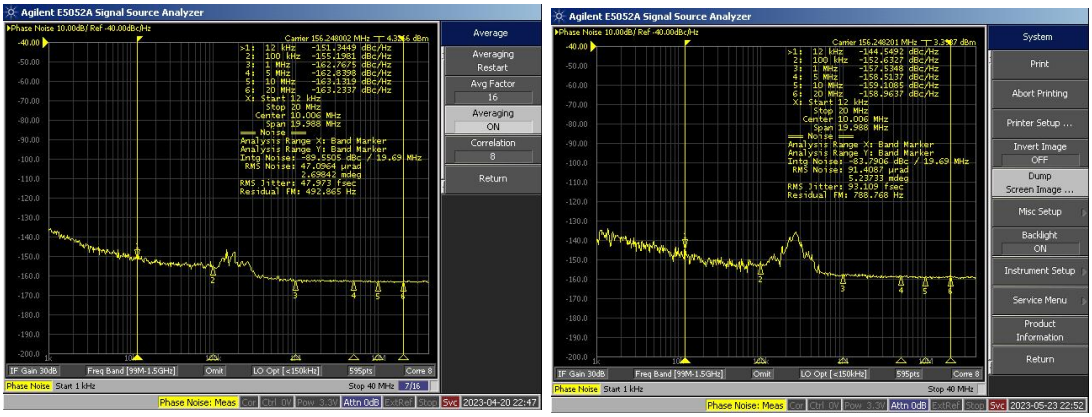
# Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns.
and at the Recommended Operation Conditions at the time of product characterization and are not ensured.(1)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Propagation Delay and Output Skew** | | | | | | |
| $t_{PD\_PECL}$ | Propagation Delay CLKin-to-LVPECL(6) | $R_T$ = 160 Ω to GND, $R_L$ = 100 Ω differential, $C_L$ ≤ 5 pF | | 0.5 | 1.5 | ns |
| $t_{SK(O)}$ | Output Skew LVPECL (4) (15) (17) | Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications. | | 20 | 50 | ps |
| $t_{SK(PP)}$ | Part-to-Part Output Skew LVPECL (6) (15) (17) | | | | 300 | ps |

(11) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

# PHASE JITTER




**(a)Jitter_Source** **(b)3V3_156M25_LVPECL**

**Figure 1 .RMS_Jitter_3V3=Sqrt(93$^2$-48$^2$)=80fs**

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

# Timing Diagrams

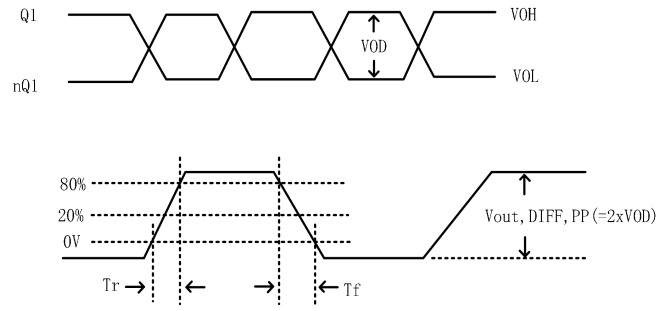
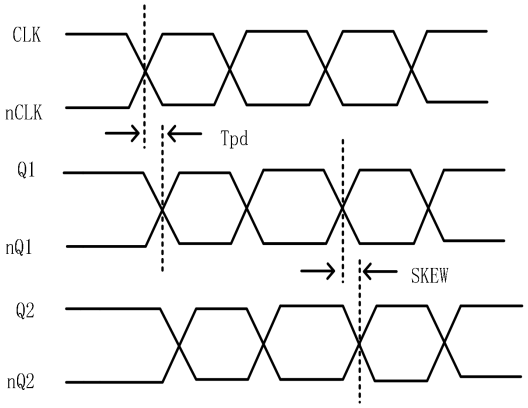



**Figure 2.output voltage and rise/fall time**




(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

**Figure 3.output and skew**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

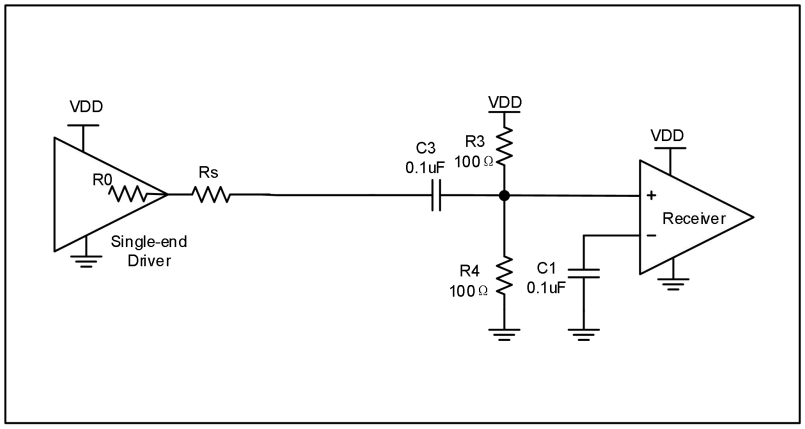
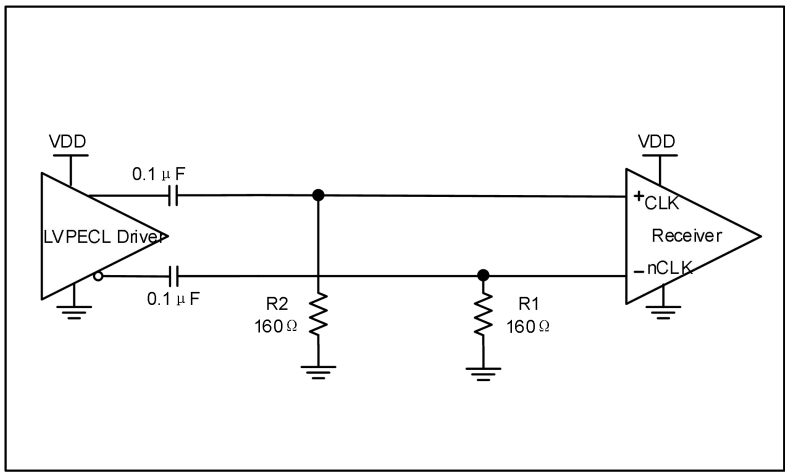
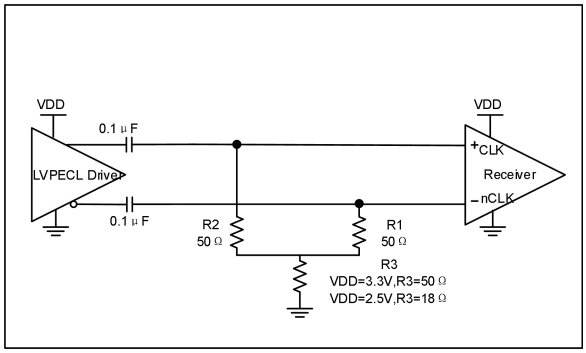


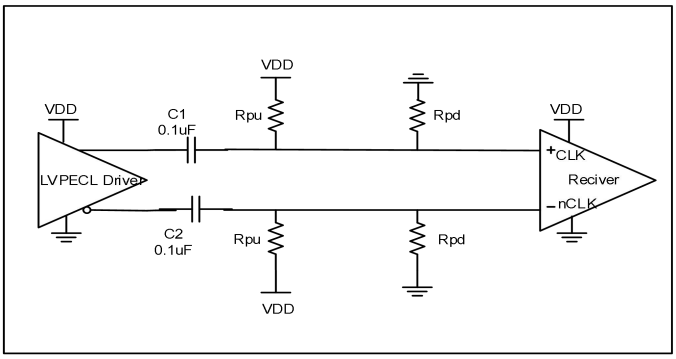

**Figure4.Single-termination method of differential input**

## Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure8 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

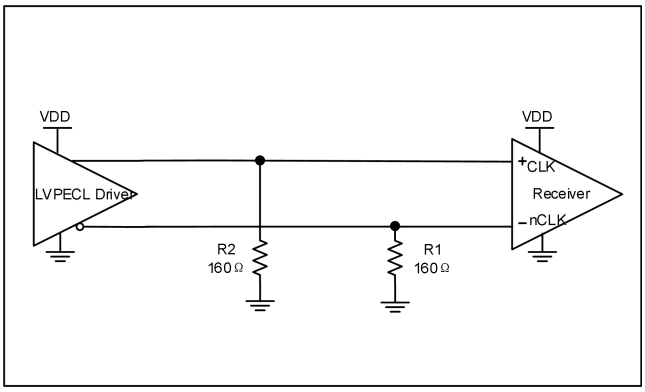


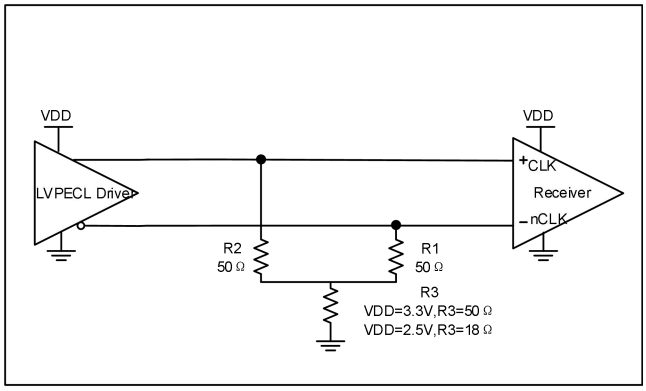


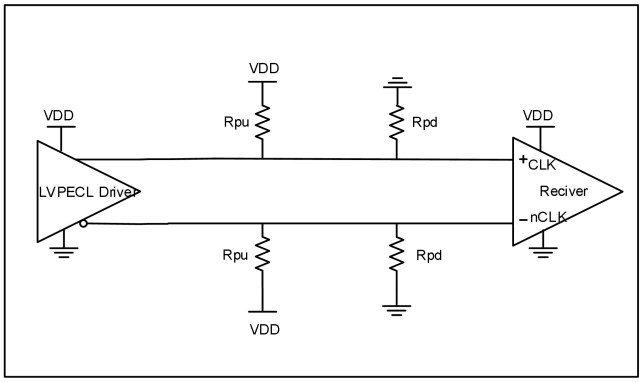




| VDD | Rpu | Rpd |
|---|---|---|
| 3.3V | 120Ω | 82Ω |
| 2.5V | 250Ω | 62.5Ω |

**Figure5.LVPECL Driver(AC)**

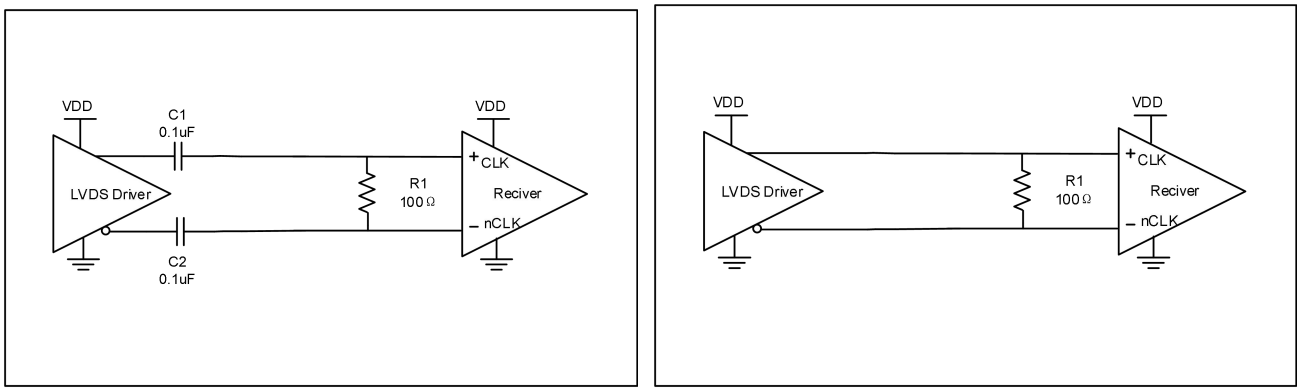


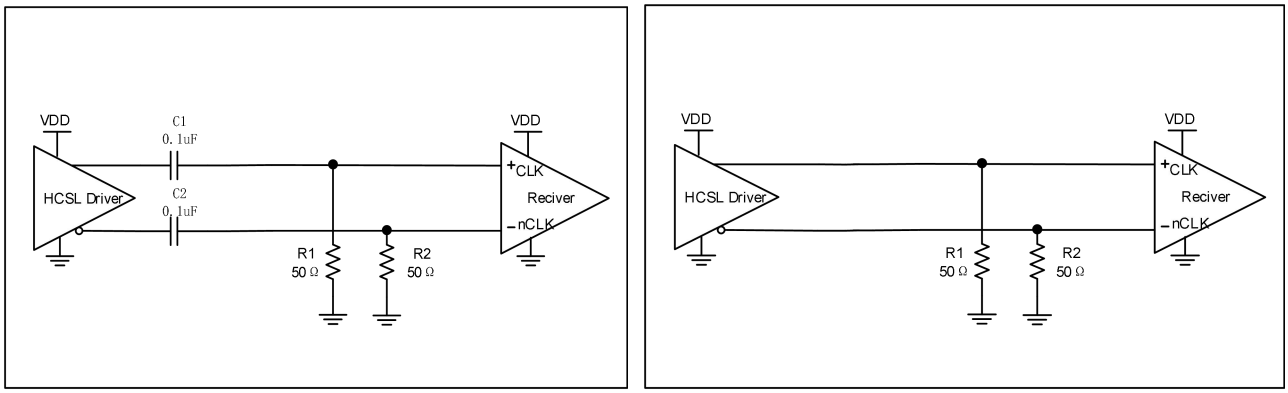

| VDD | Rpu | Rpd |
|---|---|---|
| 3.3V | 120Ω | 82Ω |
| 2.5V | 250Ω | 62.5Ω |

**Figure6.LVPECL Driver(DC)**




**a)AC coupling** **b)DC coupling**

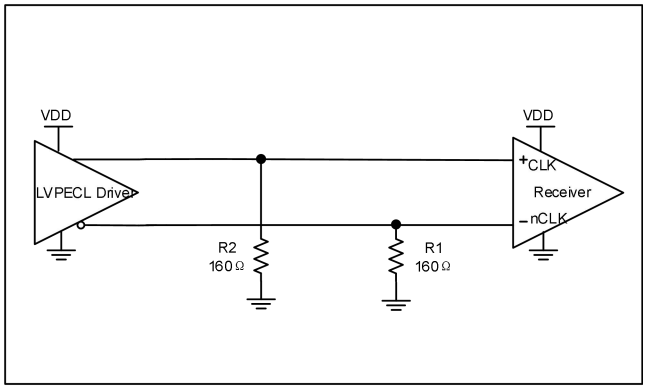
**Figure7.LVDS Driver**

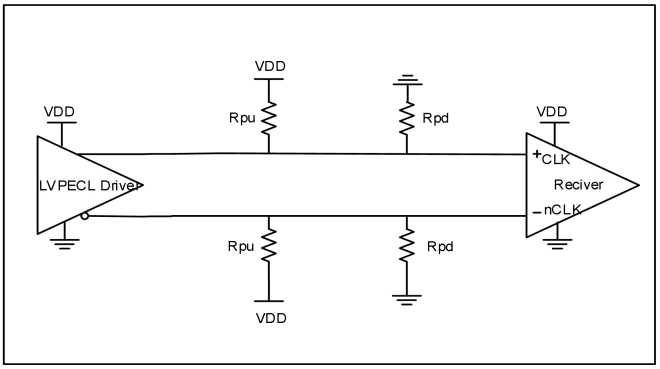



**a)AC coupling** **b)DC coupling**

**Figure8.HCSL Driver**

## Output connection circuit






| VDD | Rpu | Rpd |
|---|---|---|
| 3.3V | 120Ω | 82Ω |
| 2.5V | 250Ω | 62.5Ω |

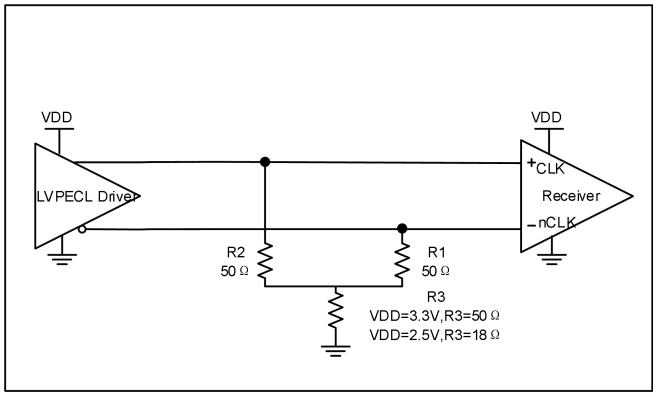
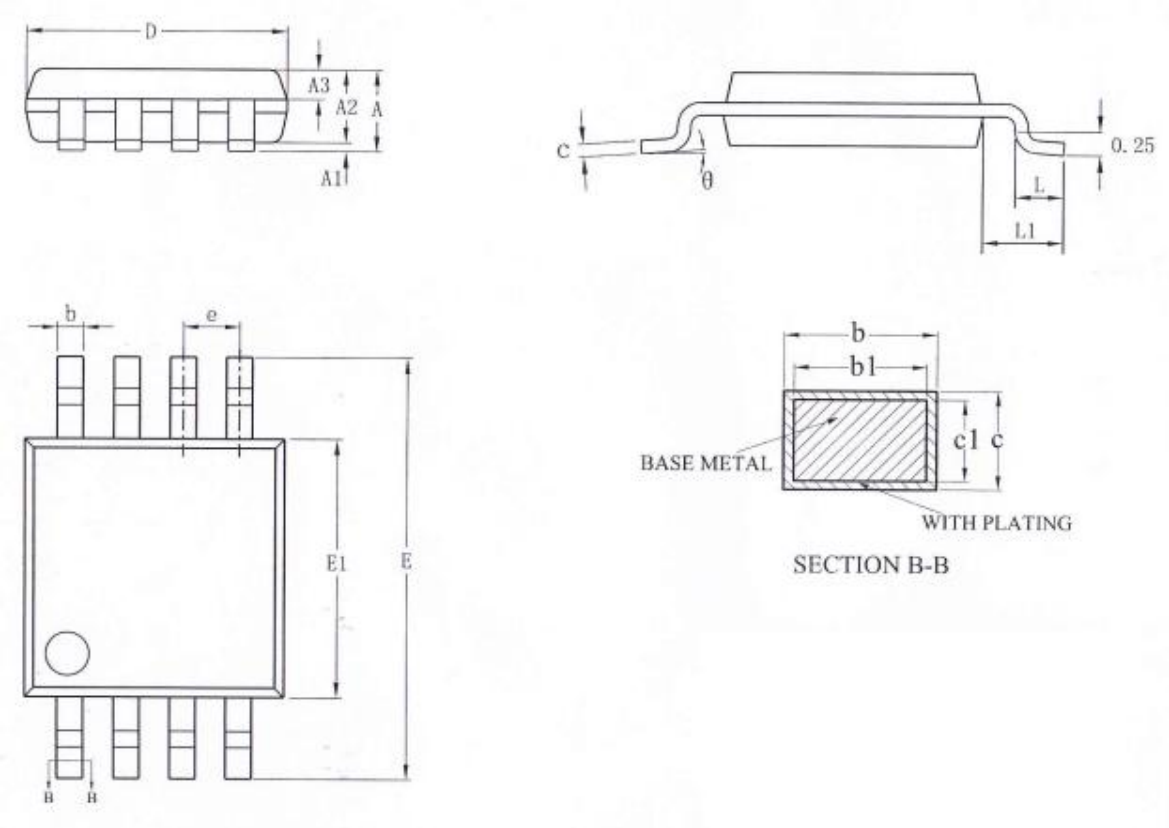



**Figure9.LVPECL Driver**

## PACKAGE DIMENSIONS




| SYMBOL | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 1.10 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| A3 | 0.30 | 0.35 | 0.40 |
| b | 0.28 | - | 0.36 |
| b1 | 0.27 | 0.30 | 0.33 |
| c | 0.15 | - | 0.19 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.90 | 3.00 | 3.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| e | 0.65BSC | | |
| L | 0.40 | - | 0.70 |
| L1 | 0.95REF | | |
| θ | 0 | - | 8° |

## Reflow profile

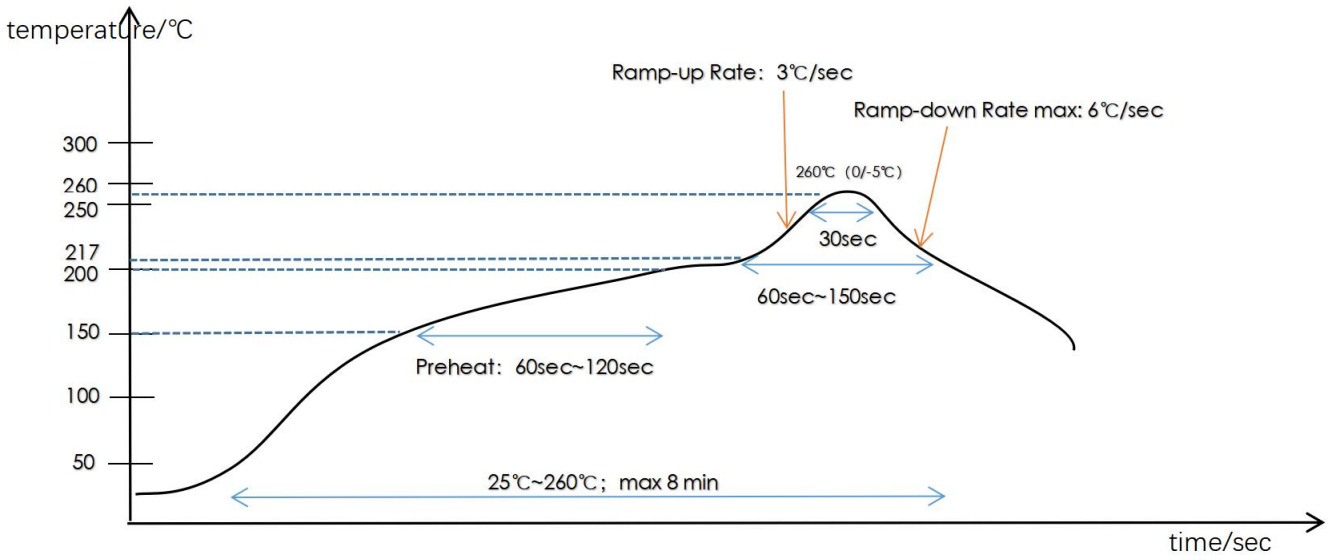



Figure10: Recommended Temperature(PB-Free)

| Reflow Condition | Convection or IR/Convection |
|---|---|
| Average ramp-up rate(217℃ to Peak) | 3℃/second max |
| Preheat temperature 175(±25)℃ | 60~120 seconds |
| Temperature maintained above 217℃ | 60~150 seconds |
| Time within 5℃ of actual peak temperature | 30 seconds |
| Peak temperature range | 260 +0/-5℃ |
| Ramp-down rate | 6℃/second max |
| Time 25℃ to peak temperature | 8 minutes max |
| Maximum number of reflow cycles | ≤3 |

## Revision History

| Date | Description of Change | Revision |
|---|---|---|
| 2023.09.25 | First Draft. | 1.0 |