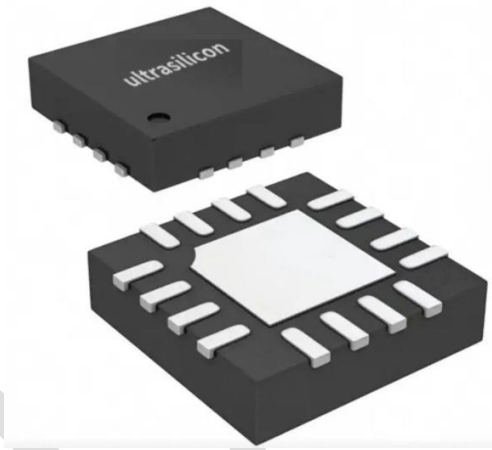
Low-Noise 5-Channl Clock Generator

US6M105Q Datasheet

Description

The US6M105Q is a low-jitter clock generator designed to provide reference clocks for communications standards such as PCI Express™. The device supports up to PCIE gen5 and is easy to configure and use. The US6M105Q provides one 125-MHz differential LVPECL clock ports and one 156.25-MHz LVPECL differential clock ports. LVPECL signaling is supported using an AC-coupled network. . Additionally, three single-ended 25-MHz clock output port is provided. Uses for this port include general-purpose clocking, clocking Ethernet PHYs, or providing a reference clock for additional clock generators. All clocks generated are derived from a single external 25-MHz crystal.



Features

- Integrated Low-Noise Clock Generator Including PLL, VCO, and Loop Filter
- 125-MHz Clocks and 156.25MHz clock ports (LVPECL)
- Bonus Single-Ended 25-MHz Output
- Integrated Crystal Oscillator Input Accepts 25-MHz Crystal
- Output Enable Pin Shuts Off Device and Outputs
- ESD Protection Exceeds 2500 V HBM, 750 V CDM,250V MM
- Industrial Temperature Range (–40°C to 85°C)
- The UltraFreq® trademark used in connection with this product
- 3.3-V Power Supply
- Small packages:
  16-pin QFN
- US6M105Q does not support spread spectrum outputs

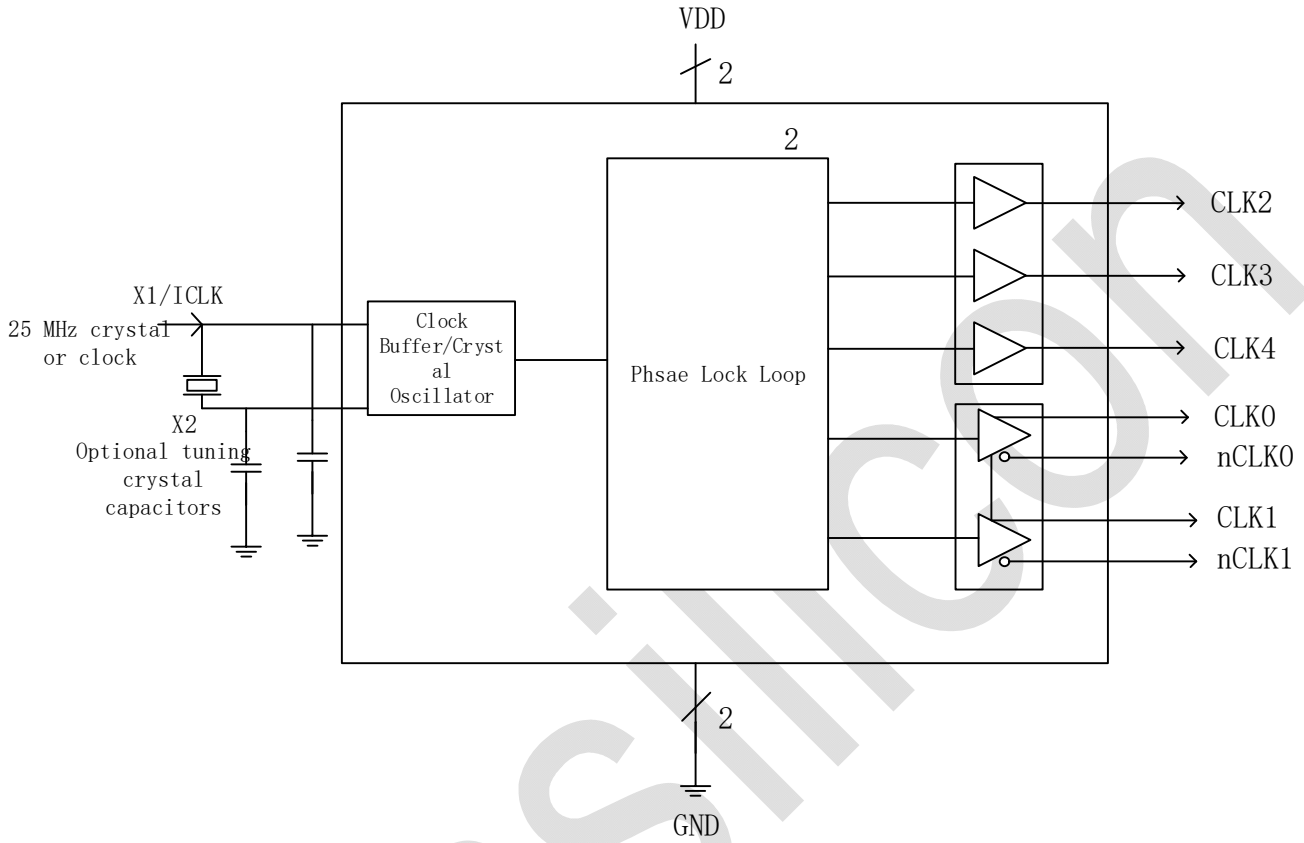
Applications

- Reference Clock Generation for PCI Express Gen 5
- General-Purpose ClockingNetwork

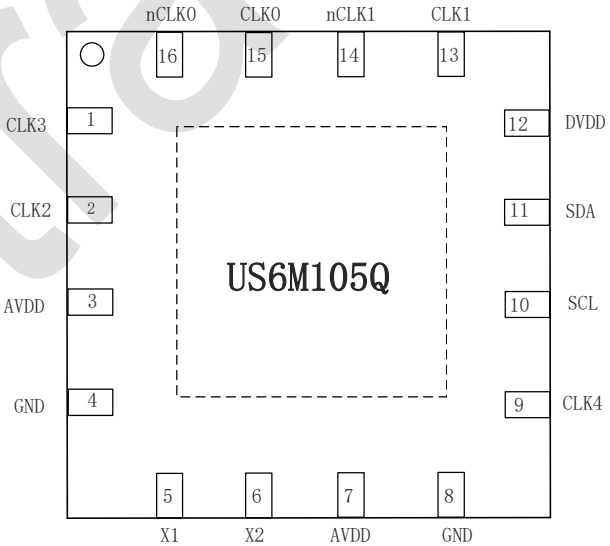
US6M105Q and subtype table

Model	Output mode		Output Frequency(MHz)
	CLK0/1、nCLK0/1	CLK2/3/4	
US6M105Q	HCSL(default)	OFF	CLK0/1:52(default)
US6M105Q-H30	HCSL	LVCMOS	CLK0: 100; CLK2/3: 25; CLK1/4: 100、25
US6M105Q-H30a	HCSL	LVCMOS	CLK1: 100; CLK2/3: 25; CLK0/4: OFF
US6M105Q-P5C0	LVPECL	LVCMOS	CLK0/1: 156.25; CLK2/3/4: 25
US6M105Q-H33	HCSL	LVCMOS	CLK0/1: 100; CLK2/3/4: 100
US6M105Q-3C0	OFF	LVCMOS	CLK2/3/4: 25; CLK0/1: OFF
US6M105Q-25125	OFF	LVCMOS	CLK2:25; CLK4:125; CLK0/1/3: OFF

Block Diagram



Pin Assignment for QFN-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Pin Description
1	CLK3	Output	LVCMOS Output 3, Typically connected to a receiver. Unused outputs can be left floating.
2	CLK2	Output	LVCMOS Output 2, Typically connected to a receiver. Unused outputs can be left floating.
3	AVDD	Power	Connect to voltage supply +3.3 V.
4	GND	Power	Connect to ground.
5	X1	Input	Crystal or clock input. Connect to a 25 MHz crystal or single ended clock.
6	X2	Output	Crystal connection. Leave unconnected for clock input.
7	AVDD	Power	Connect to voltage supply +3.3 V.
8	GND	Power	Connect to ground.
9	CLK4	Output	LVCMOS Output 4, Typically connected to a receiver. Unused outputs can be left floating.
10	SCL	-	Serial Clock Input.
11	SDA	-	Serial Data Input/Output.
12	DVDD	Power	Connect to voltage supply +3.3 V.
13	CLK1	Output	LVPECL true clock output 1.
14	nCLK1	Output	LVPECL complementary clock output 1.
15	CLK0	Output	LVPECL true clock output 0.
16	nCLK0	Output	LVPECL complementary clock output 0.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 uF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the US6M105 to meet PCI Express specifications.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	3.3V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V

Electrical Characteristics

VDD = 3.3 V ±5% and TA = –40°C to 85°C (unless otherwise noted).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Input						
Input Frequency	F_{IN}			25		MHz
Singel ended output for VDD = 3.3 V ± 5%						
Output High Voltage	V_{OH}		2.8			V
Output Low Voltage	V_{OL}				0.2	
Rise Time	T_{OR}	From 20% to 80%, 156.25MHz		160	300	ps
		From 20% to 80%, 125MHz		220	300	
Fall Time	T_{OF}	From 80% to 20%, 156.25MHz		160	300	
		From 80% to 20%, 125MHz		220	300	
Output Skew	Skew	VDD=3.3V@100MHz		30	50	ps
phase jitter	$T_{jitter-ADD}$	12kHz to 20MHz@156.25MHz	—	330	—	fs
		12kHz to 20MHz@125MHz	—	400	—	
LVPECL Clocks						
Output Frequency	F_{OUT}		—	156.25	—	MHz
			—	125	—	MHz
Output High Voltage	V_{OH}	VDD = 3.3V	—	2260	—	mV
Output Low Voltage	V_{OL}		—	1230	—	mV
Crossing Point Voltage	V_{OX}	Absolute	—	1700	—	mV
Frequency Accuracy	FACC	All output clocks	—	—	80	ppm
Slew Rate	TR/TF	Measured differentially from ±150 mV			4.0	V/ns
Cycle-to-Cycle Jitter	TCCJ	Measured at 0 V differential	—	28	70	ps
PCIe Phase Jitter Common Clocked Architecture	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s)	—	70	90	fs
Rise Time	T_{OR}	From 20% to 80%, 156.25MHz	—	130	300	ps
		From 20% to 80%, 125MHz		130	300	
Fall Time	T_{OF}	From 80% to 20%, 156.25MHz	—	120	300	ps
		From 80% to 20%, 125MHz		120	300	
Duty Cycle			45	—	55	%
Output Skew	Skew	VDD=3.3V		30	50	ps
phase jitter	$T_{jitter-ADD}$	12kHz to 20MHz@156.25MHz	—	221	300	fs
		12kHz to 20MHz@125MHz	—	227	300	
Enable/Disable and Set-up						
Clock Stabilization from Power-	TSTABLE		—	—	3	ms
Stopclock Set-up Time	TSS		10.0	—	—	ns

Applications Information

Single-termination method

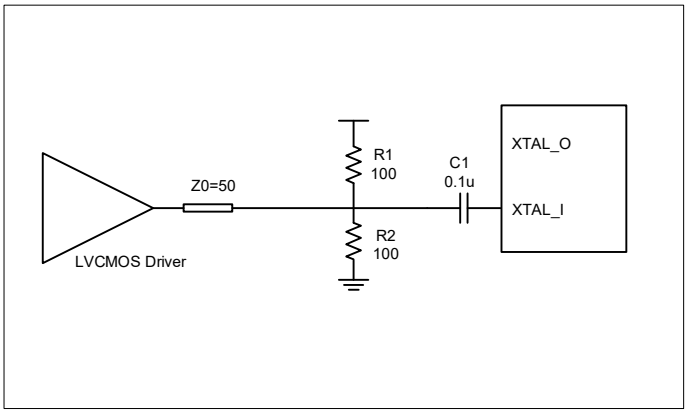
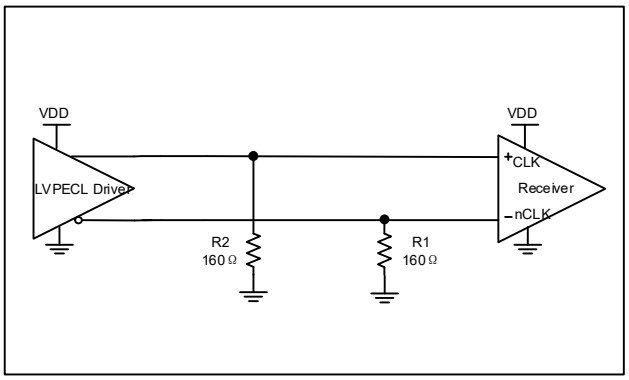
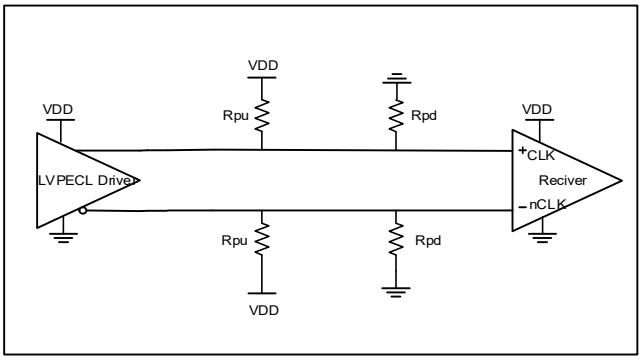


Figure1.Single-termination input

Output connection circuit





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

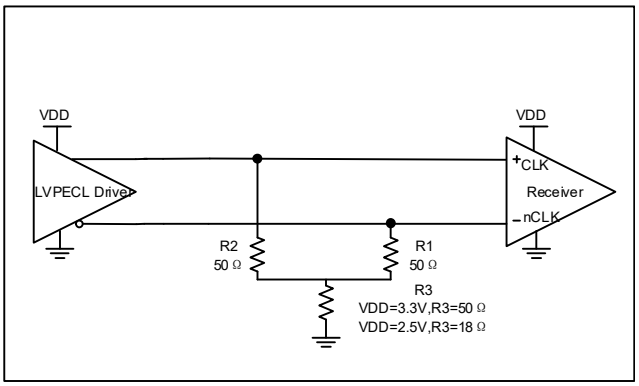
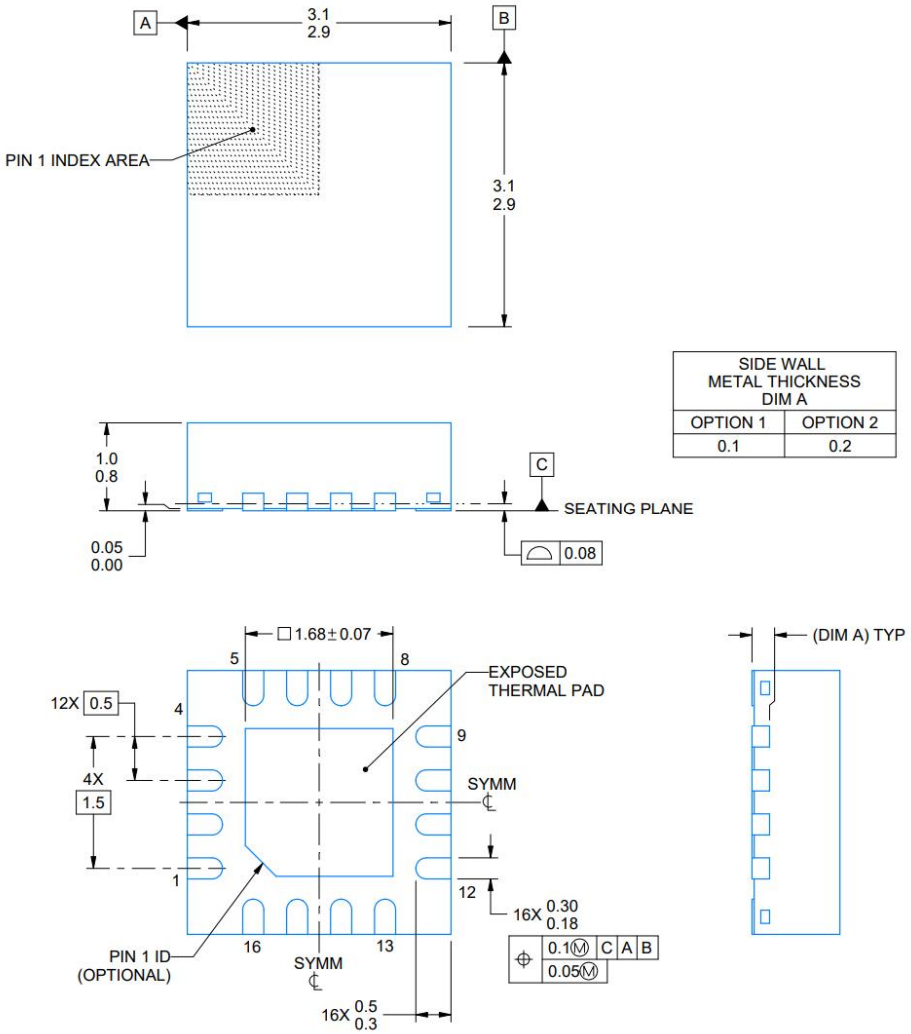


Figure2.LVPECL Driver

PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

Reflow profile

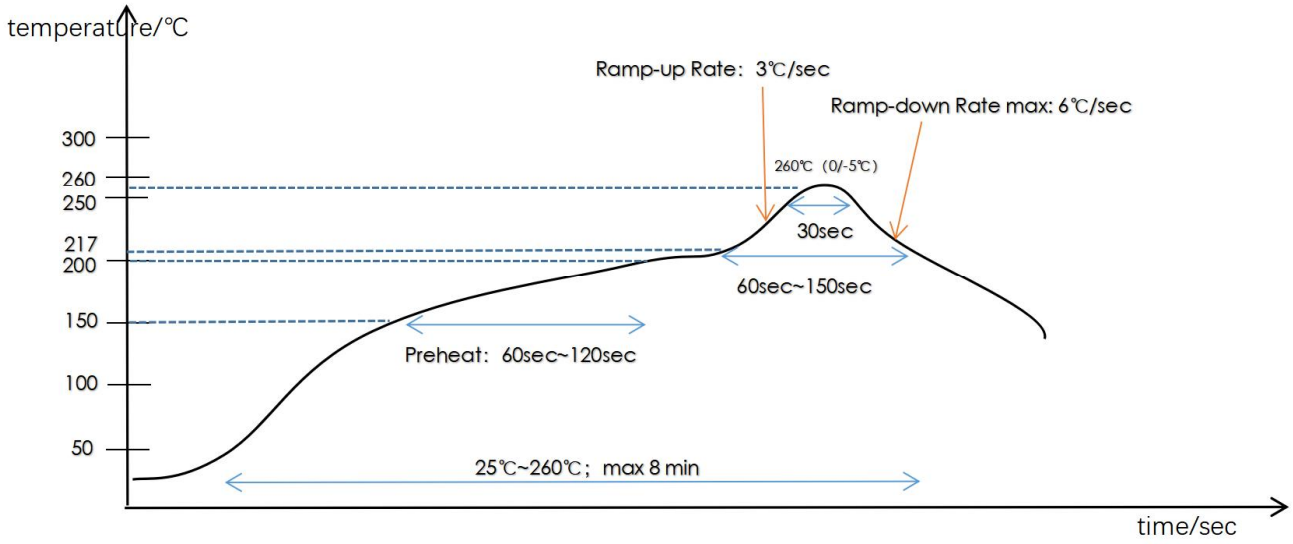


Figure3: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.3.6	First Draft.	1.0
2024.7.18	Modify the chip package diagram.	1.5
2024.7.30	Add the submodel table.	2.0
2025.9.29	Modify the pin assignment	2.5
2026.1.23	Add product trademark.	3.0
2026.6.9	Modify the submodel table.	3.5