US5S108FN 1.8V, 2.5V, 3.3V LVCMOS Clock Buffer

Description

The US5S108FN is a low skew, single input to eight output, clock buffer.

This device has high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from –40°C to 85°C.

Applications

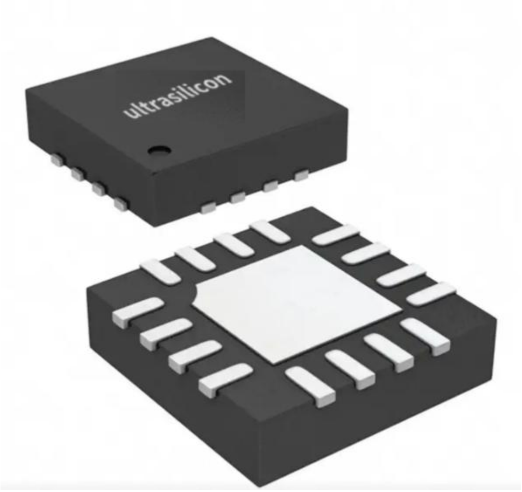
- General-Purpose Communication, Industrial, and Consumer Applications

Device Information

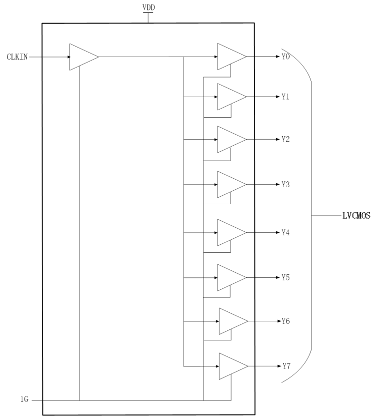
Part Number	Package	Body Size(NOM)
US5S108FN	QFN-16	2.5mm x 2.5mm

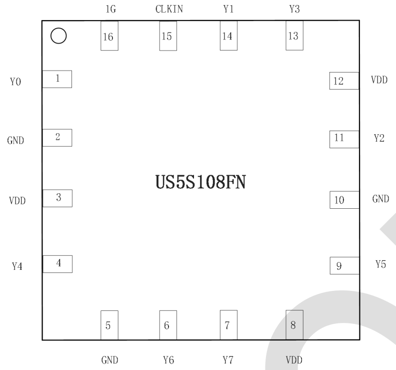
Features

- High-Performance 1:8 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 55 ps (Typical)
- Very low propagation delay < 3 ns
- Synchronous Output Enable Is Available
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range: -40°C to 85°C
- Available in QFN 2.5mmX2.5mm Package



Block Diagram





Pin Description and Function Table

Pin Descriptions

Number	Name	Type	Description
1	Y0	Output	LVCMOS output 0. Typically connected to a receiver. Unused outputs can be left floating.
2	GND	Power	Ground.
3	VDD	Power	DC power supply,1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-μF capacitor near the pin.
4	Y4	Output	LVCMOS output 4. Typically connected to a receiver. Unused outputs can be left floating.
5	GND	Power	Ground.
6	Y6	Output	LVCMOS output 6. Typically connected to a receiver. Unused outputs can be left floating.
7	Y7	Output	LVCMOS output 7. Typically connected to a receiver. Unused outputs can be left floating.
8	VDD	Power	DC power supply,1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-μF capacitor near the pin.
9	Y5	Output	LVCMOS output 5. Typically connected to a receiver. Unused outputs can be left floating.
10	GND	Power	Ground.
11	Y2	Output	LVCMOS output 2. Typically connected to a receiver. Unused outputs can be left floating.
12	VDD	Power	DC power supply,1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-μF capacitor near the pin.
13	Y3	Output	LVCMOS output 3. Typically connected to a receiver. Unused outputs can be left floating.
14	Y1	Output	LVCMOS output 1. Typically connected to a receiver. Unused outputs can be left floating.
15	CLKIN	Input	Single-ended clock input with internal 150-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
16	1G	Input	Global Output Enable with internal 50-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled

Output Logic Table

Inputs		Outputs
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	0.5V to 3.6V
V_{CLKIN} : Input voltage (CLKIN)	
V_{IN} : Input voltage (1G)	
V_{Yn} : Output pins (Yn)	-0.5V to V_{DD} + 0.3 V
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40	-	85	°C
T_J	Junction temperature		-	125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5% 1.8-5%	3.3 2.5 1.8	3.3+5% 2.5+5% 1.8+5%	V

Electrical Characteristics

VDD = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Core supply current	All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 1.8 V		20		mA
		All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 2.5 V		27		
		All-outputs active, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 3.3 V		37		
CLOCK INPUT						
f_{IN_SE}	Input frequency	V_{DD} = 3.3 V	0.1		250	MHz
		V_{DD} = 2.5 V and 1.8 V	0.1		200	
V_{IH}	Input high voltage		0.7 x V_{DD}			V
V_{IL}	Input low voltage				0.3 x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I_{IN_LEAK}	Input leakage current		–50		50	uA
C_{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V_{DD} LEVELS						
f_{OUT}	Output frequency	VDD = 3.3 V	0.1		250	MHz
		VDD = 2.5 V and 1.8 V	0.1		200	
O_{DC}	Output duty cycle	With 50% duty cycle input	45		55	%
t_{START}	Start-up time before output is active	See (1)			3	ms
t_{1G_ON}	Output enable time	See (2)			5	cycles
t_{1G_OFF}	Output disable time	See (3)			5	cycles
CLOCK OUTPUT FOR V_{DD} = 3.3 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = -8 mA	2.6			V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.5	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.35	0.7	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)		25	50	ps
$t_{PART-SKEW}$	Part-to-part skew				450	
$t_{PROPDELAY}$	Propagation delay	See (5)		1.5	2	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		20	35	fs, RMS
R_{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V_{DD} = 2.5 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = -8 mA	1.9			V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.5	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.33	0.8	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4			50	ps
$t_{PART-SKEW}$	Part-to-part skew				400	
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	2.5	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		25	45	fs, RMS
R_{OUT}	Output impedance			50		Ω

(1) Measured from VDD stable to output active, when 1G = HIGH.
(2) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
(3) Measured from 1G falling edge crossing VIL to last falling edge of Yn.

(4) Measured from rising edge of any Yn output to any other Ym output.
(5) Measured from rising edge of CLKIN to any Yn output.

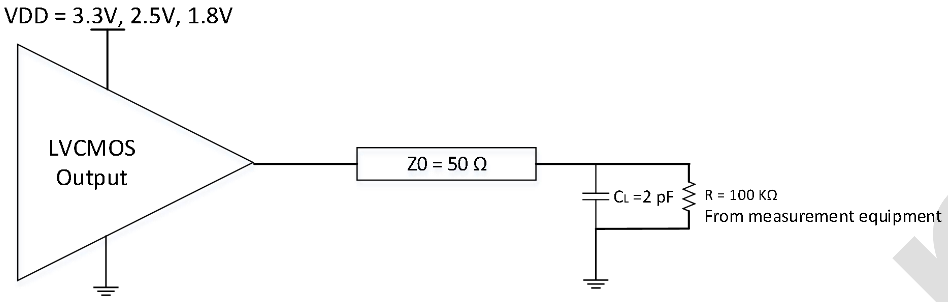
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT FOR V_{DD} = 1.8 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = -8 mA	1.2			V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.5	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.38	1	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)			50	ps
$t_{PART-SKEW}$	Part-to-part skew				900	ps
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	3	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		55	85	fs, RMS
R_{OUT}	Output impedance			50		Ω
GENERAL PURPOSE INPUT (1G)						
V_{IH}	High-level input voltage		0.7 x V_{DD}			V
V_{IL}	Low-level input voltage				0.3 x V_{DD}	
I_{IH}	Input high-level current	V_{IH} = V_{DD_REF}			67	μA
I_{IL}	Input low-level current	V_{IL} = GND			1	

Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C

Power Supply		Min	Typ	Max	Unit
V/t_{RAMP}	V_{DD} ramp rate	0.1	-	50	V/rms

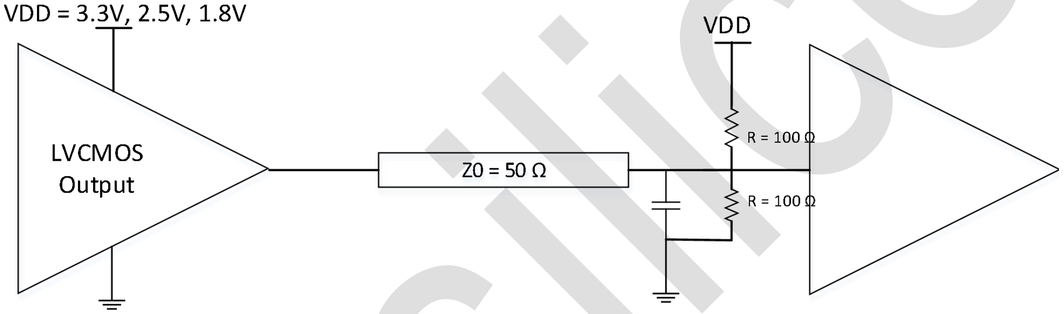
Parameter Measurement Information



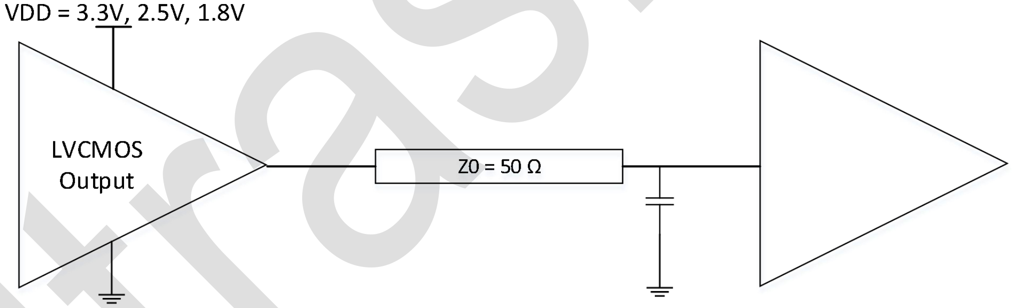
Test Load Circuit

Note:

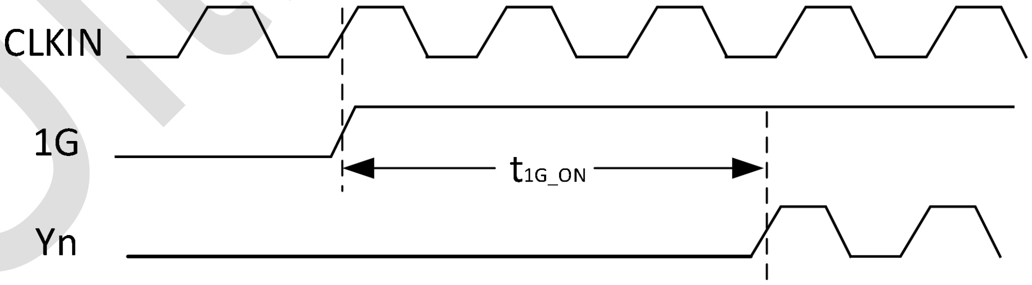
1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency ⩽ 250MHz, Z_O = 50 Ω, tr < 1.2ns, tf < 1.2ns



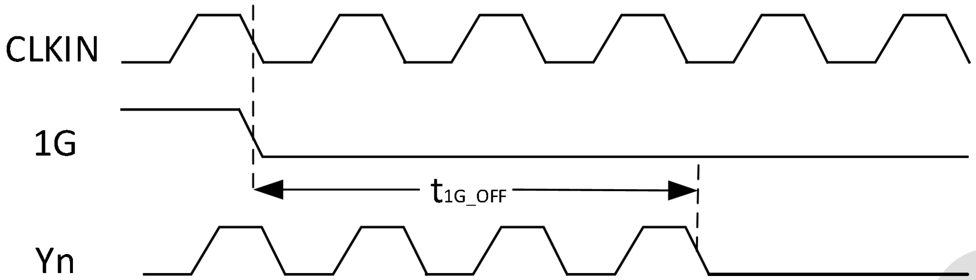
Application Load With 50-Ω Termination



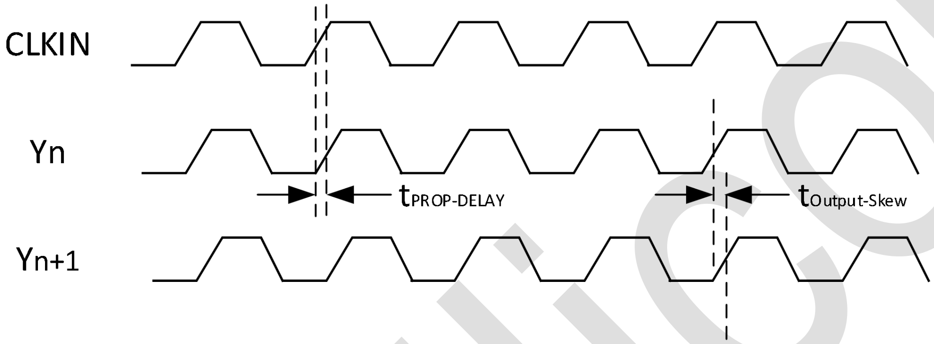
Application Load With Termination



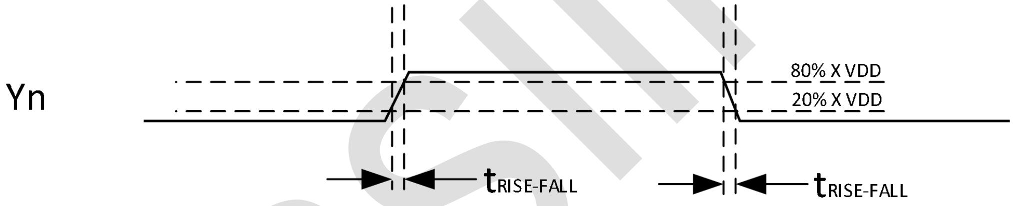
T_{1G_ON} Output Enable Time



T_{1G_OFF} Output Enable Time

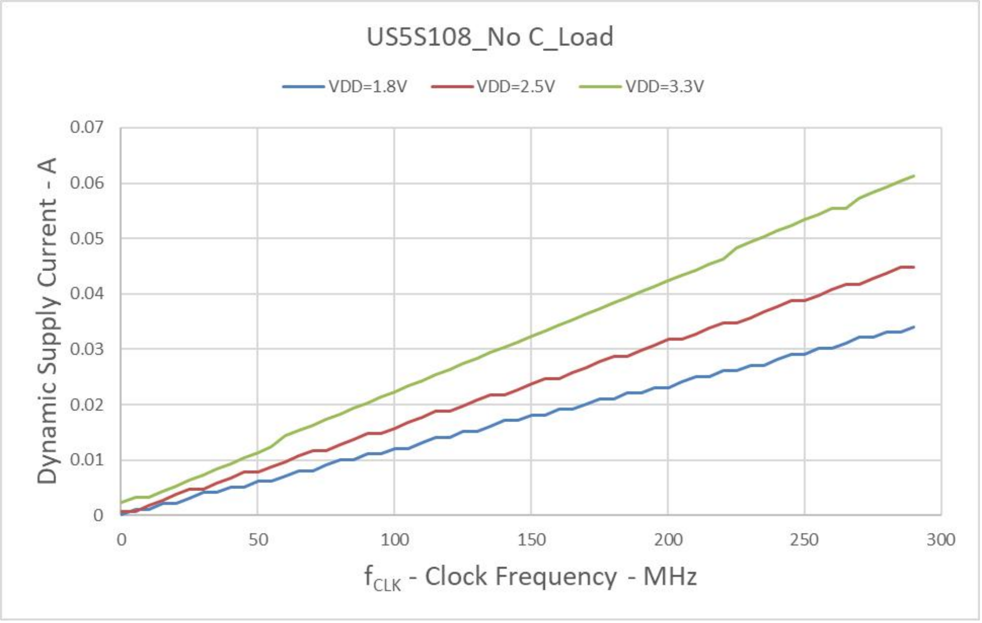


Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$

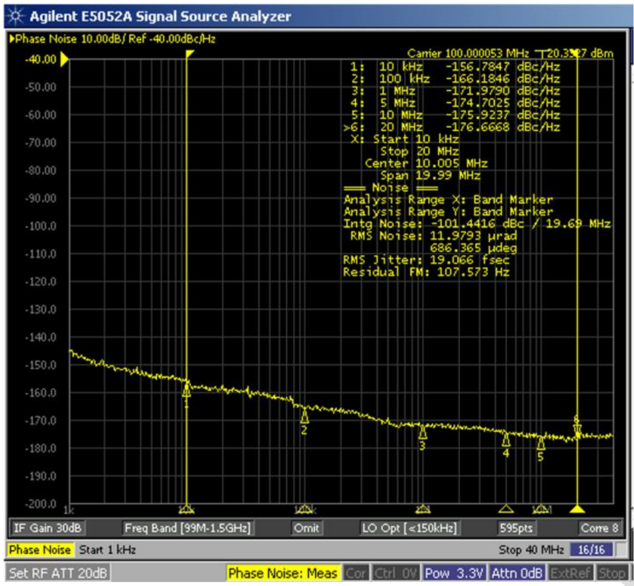


Rise and Fall Time $t_{RISE-FAIL}$

Dynamic Supply Current vs. Clock Frequency

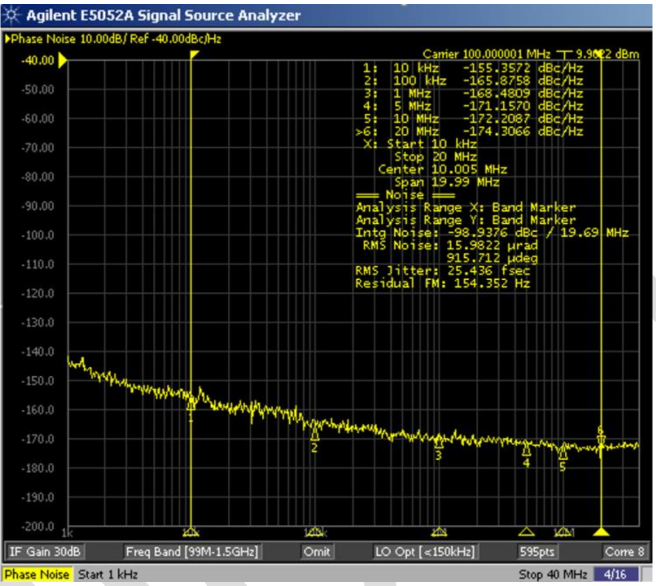


Phase Noise Plot



```
Carrier 100.000053 MHz   20.3[illegible]27 dBm
  1:  10 kHz   -156.7847 dBc/Hz
  2:  100 kHz  -166.1846 dBc/Hz
  3:  1 MHz    -171.9790 dBc/Hz
  4:  5 MHz    -174.7025 dBc/Hz
  5:  10 MHz   -175.9237 dBc/Hz
>6:  20 MHz   -176.6668 dBc/Hz
  X: Start 10 kHz
      Stop 20 MHz
    Center 10.005 MHz
      Span 19.99 MHz
═══ Noise ═══
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -101.4416 dBc / 19.69 MHz
 RMS Noise: 11.9793 µrad
            686.365 µdeg
RMS Jitter: 19.066 fsec
Residual FM: 107.573 Hz
```

Wenzel 100MHz OCXO(19fs)

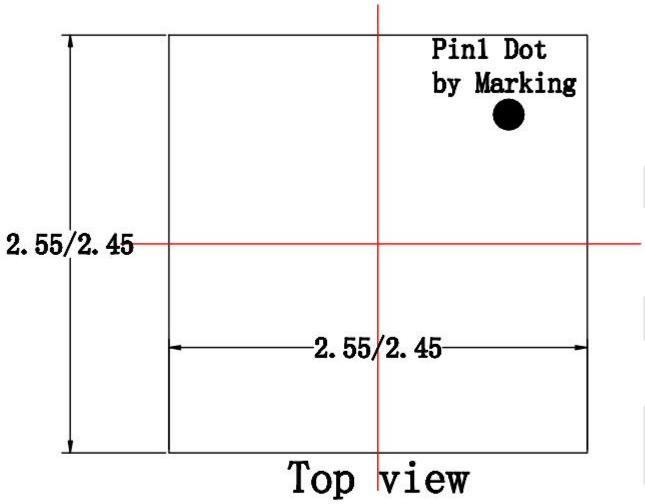


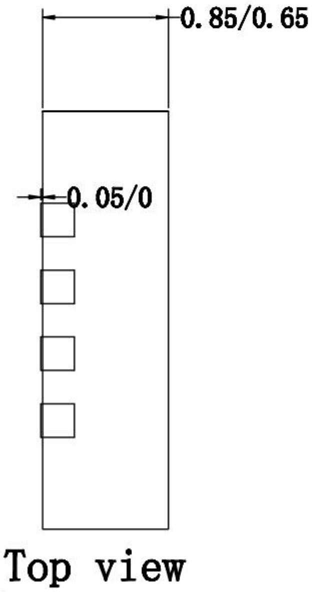
```
Carrier 100.000001 MHz   9.9[illegible]2 dBm
  1:  10 kHz   -155.3572 dBc/Hz
  2:  100 kHz  -165.8758 dBc/Hz
  3:  1 MHz    -168.4809 dBc/Hz
  4:  5 MHz    -171.1570 dBc/Hz
  5:  10 MHz   -172.2087 dBc/Hz
>6:  20 MHz   -174.3066 dBc/Hz
  X: Start 10 kHz
      Stop 20 MHz
    Center 10.005 MHz
      Span 19.99 MHz
═══ Noise ═══
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -98.9376 dBc / 19.69 MHz
 RMS Noise: 15.9822 µrad
            915.712 µdeg
RMS Jitter: 25.436 fsec
Residual FM: 154.352 Hz
```

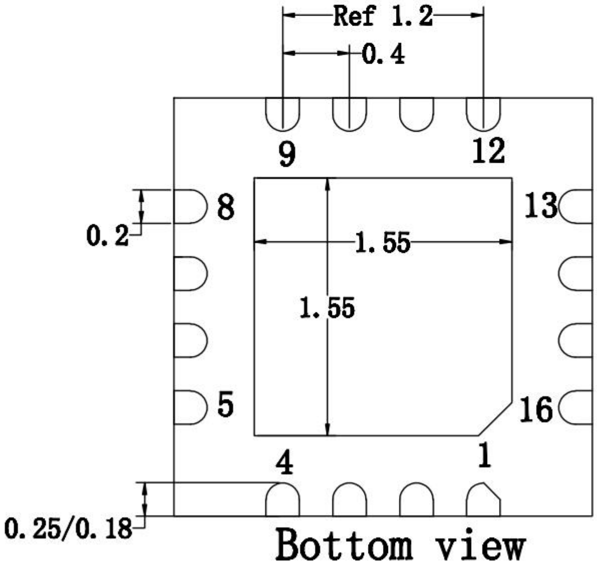
US5S108 Ouput Phase Noise(25.5fs)

The additive phase jitter for this device was measured using the Wenzel 100MHz OCXO(19fs) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

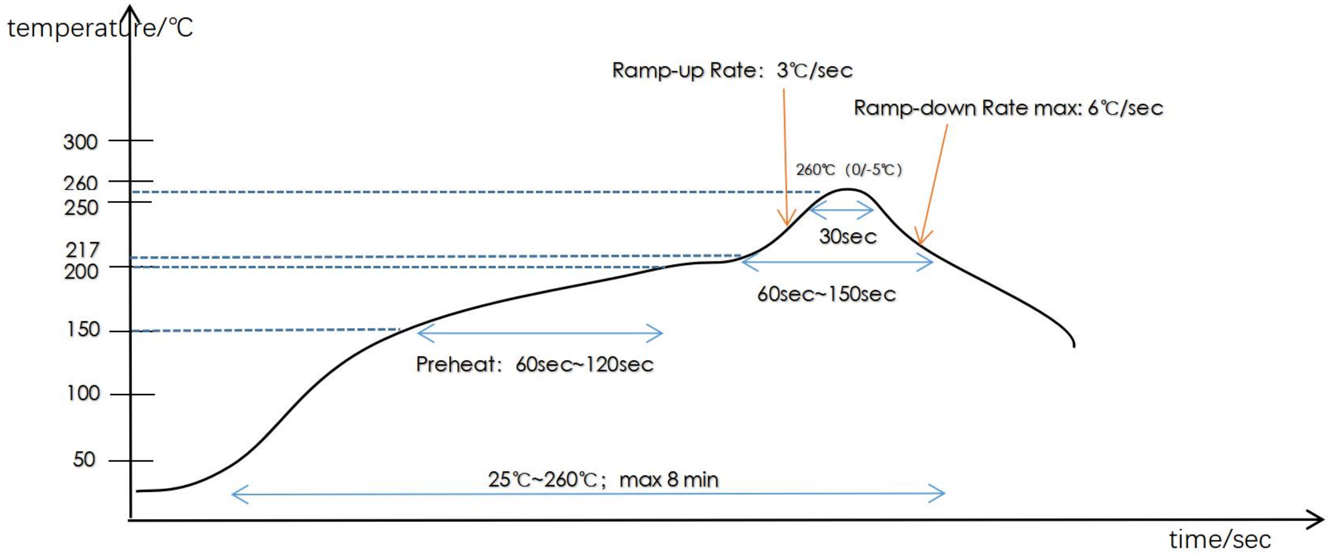
PACKAGE DIMENSIONS







Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0
2023.02.10	Operating frequency range change。	1.5
2024.01.12	Add ePAD to dimension diagram	2.0