Description

US6D102-H3 belongs to our clock generator, is a member of high-performance PCIe clock generator family.H3 in US6D102-H3 represents that the output frequency supports 100MHz. See Table1.

Table 1. output frequency represented by H3

CH0		CH1	
100MHz	HCSL	100MHz	HCSL

US6D102-H3 is a high-performance, PCIe clock generator that can source two PCIe clocks from a 25 MHz crystal or clock input. The clock outputs are compliant to PCIe Gen 5 common clock, and Gen 5 SRNS specifications. The ultra-small footprint and industry leading low power consumption make US6D102-H3 the ideal clock solution for applications with tight board space constraints.

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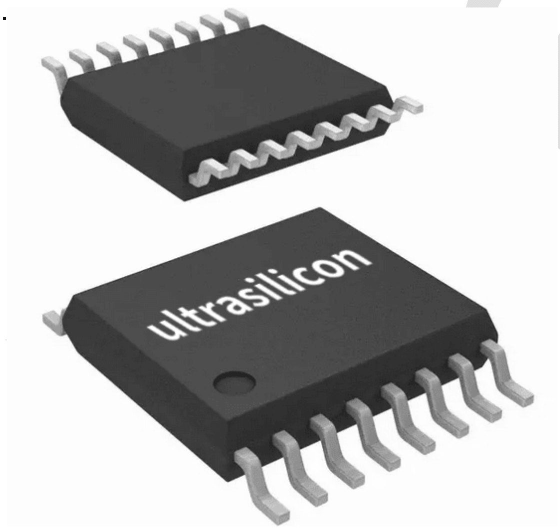


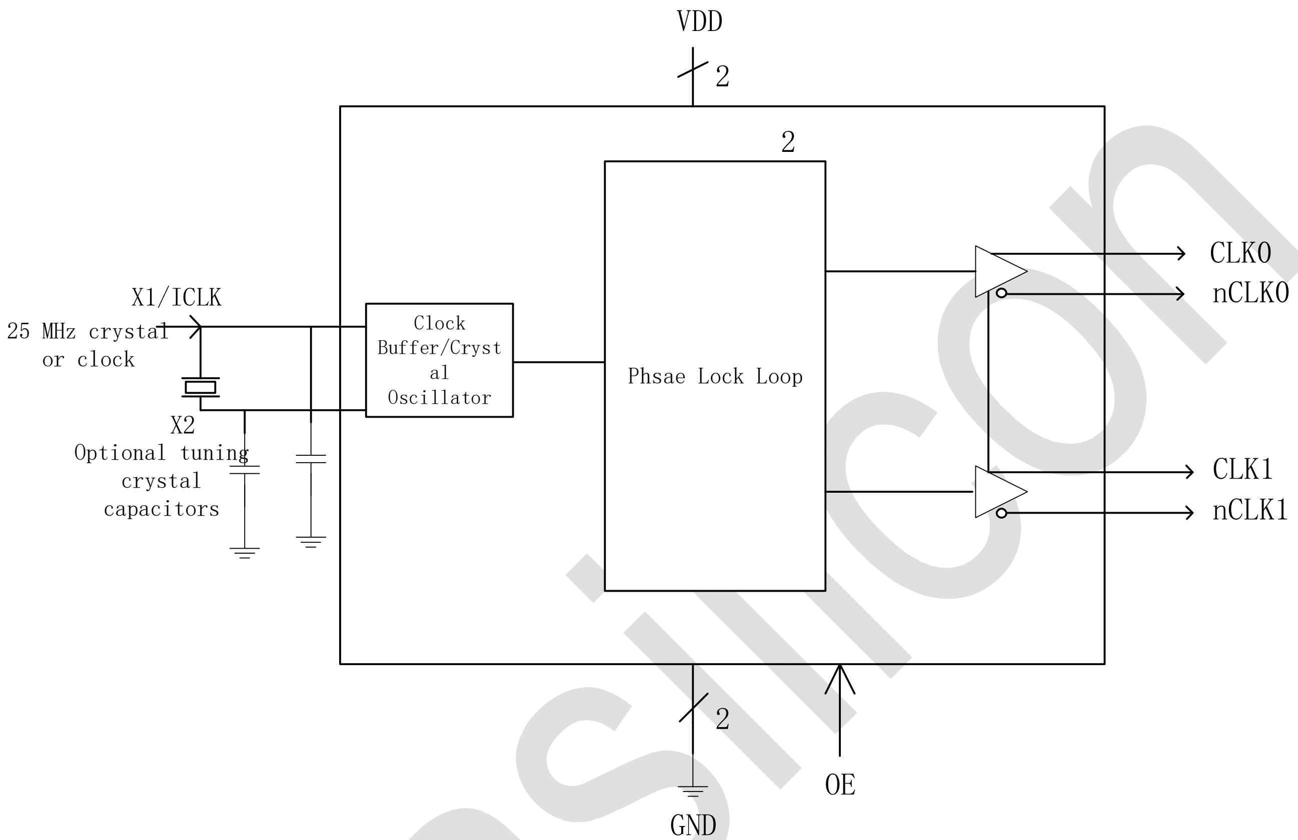
Features

- 2 output synthesizer for PCIe Gen1/2/3/4/5 and Ethernet
- 2 Non-spread 0.7V current mode differential HCSL output pairs
- OE control pin; greater system power management
- supports demanding embedded applications
- Industrial Temperature Range: -40°C to 85°C
- Output-to-output skew <50 ps
- Low phase noise@100MHz: 12kHz to 20MHz <300 fs RMS
- The UltraClock® trademark used in connection with this product
- Small packages:
  16-pin TSSOP
- US6D102-H3 does not support spread spectrum outputs

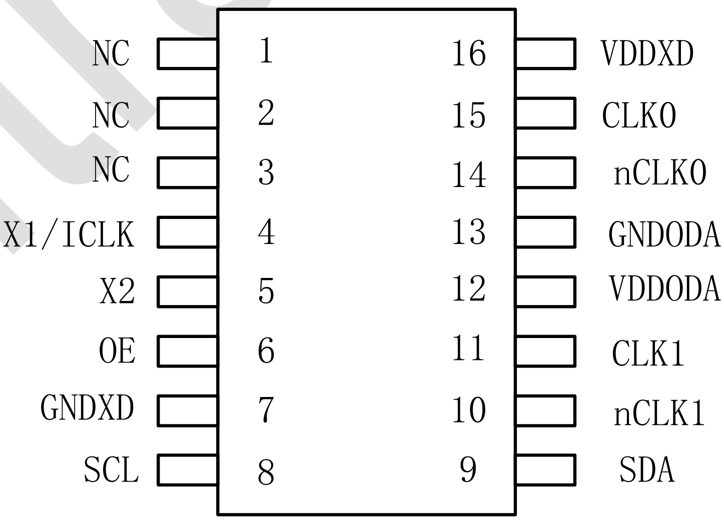
Applications

- Network attached storage
- Multi-function printer
- PCIe Add-on Cards
- Network Interface Cards
- Docking Stations
- Wireless access point
- Routers
- Digital Still Cameras
- Digital Video Cameras

Block Diagram



Pin Description and Function Table



Number	Name	Type	Pin Description
1	NC	-	No Connect
2	NC	-	No Connect
3	NC	–	No connect.
4	X1/ICLK	Input	Crystal or clock input. Connect to a 25 MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable. Tristates outputs and device is not shut down. Internal 100-kΩ pull-up resistor.
7	GNDXD	Power	Connect to ground.
8	SCL	-	Serial Clock Input.
9	SDA	-	Serial Data Input/Output.
10	nCLK1	Output	HCSL clock output 1.
11	CLK1	Output	HCSL clock output 1.
12	VDDODA	Power	Connect to voltage supply +3.3 V or 2.5V for output driver and analog circuits
13	GNDODA	Power	Connect to ground.
14	nCLK0	Output	HCSL clock output 0.
15	CLK0	Output	HCSL clock output 0.
16	VDDXD	Power	Connect to voltage supply +3.3 V or 2.5V for crystal oscillator and digital circuit.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 uF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the US6D102-H3 to meet PCI Express specifications.

Table 1. Absolute Maximum Conditions

Item	Rating
V_{DD}, V_{DDOX}[1]	4.6V
V_{IN}	-0.3V to V_{DDOX}[1] + 0.3V
T_J :Junction Temperature	150°C
T_{STG} :Storage Temperature	-65°C to 150°C

Table 2. ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Electrical Specifications

Table 3. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	3.3 V ± 5% 2.5 V ± 5%	3.13 2.375	3.3 2.5	3.46 2.625	V
Operating Supply Current	I_{DD}	Full Active	—	24.3	—	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Table 4. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Input						
Input Frequency	F_{IN}			25		MHz
HCSL Clocks						
Output Frequency	F_{OUT}		—	100	—	MHz
Output High Voltage	V_{OH}	VDD = 3.3V	660	700	850	mV
Output Low Voltage	V_{OL}		-150	0	27	mV
Crossing Point Voltage	V_{OX}	Absolute	250	350	550	mV
Crossing Point Voltage	V_{CN}	Variation over all edges			140	mV
Frequency Accuracy	F_{ACC}	All output clocks	—	—	30	ppm
PCIe Phase Jitter Common Clocked Architecture	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen5 (32.0 GT/s)	—	70	90	fs
phase jitter		12kHz to 20MHz@100MHz,VDD=3.3V			300	fs
Rise Time	T_{OR}	From 20% to 80%		220	500	ps
Fall Time	T_{OF}	From 80% to 20%		220	500	ps
Duty Cycle			45		55	%
Enable/Disable and Set-up						
Clock Stabilization from Power-	T_{STABLE}		—	—	3	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Crystal Recommendations

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using two trim capacitors.

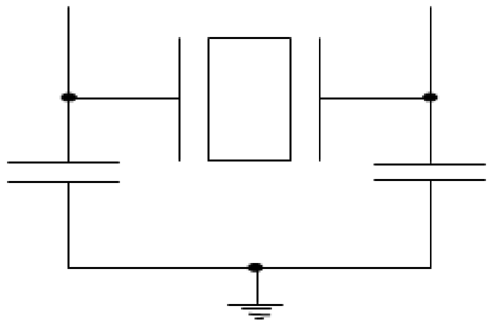


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

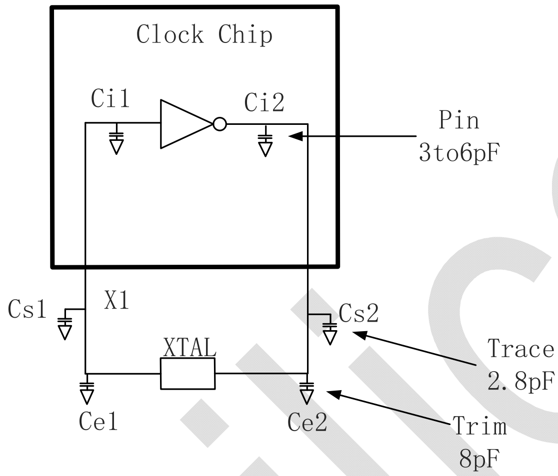


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci: Internal capacitance (lead frame, bond wires, etc.

Phase Jitter

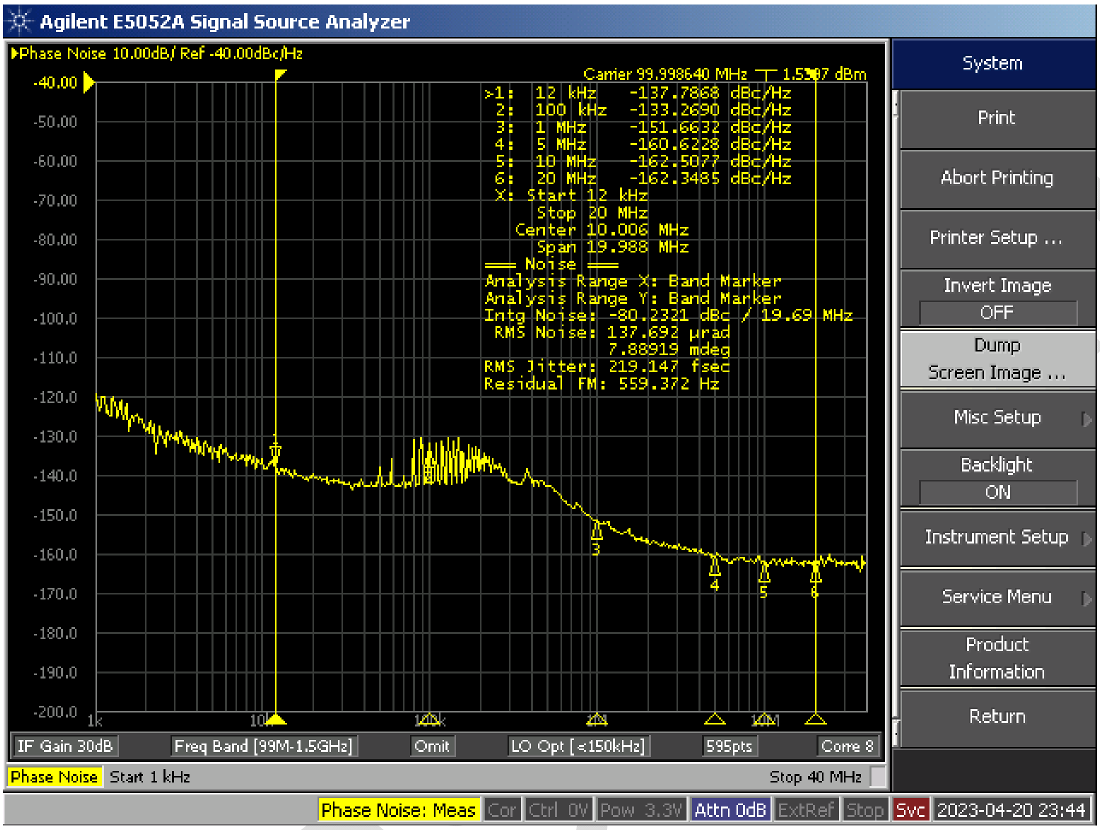


Figure 3. Phase Jitter @100MHz（RMS 12kHz to 20MHz）

Applications Information

Single-termination method:

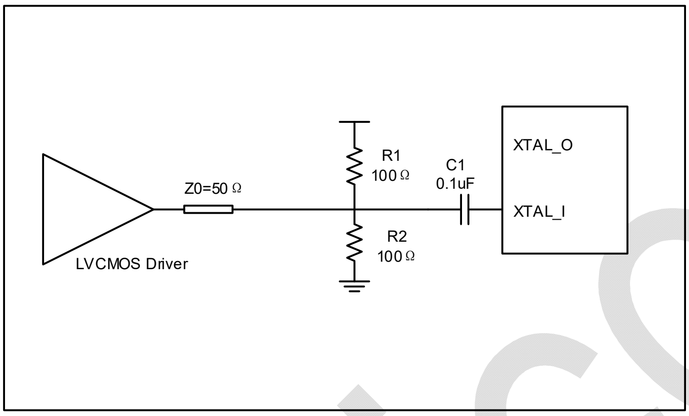


Figure 4.Single-ended output

Output connection circuit:

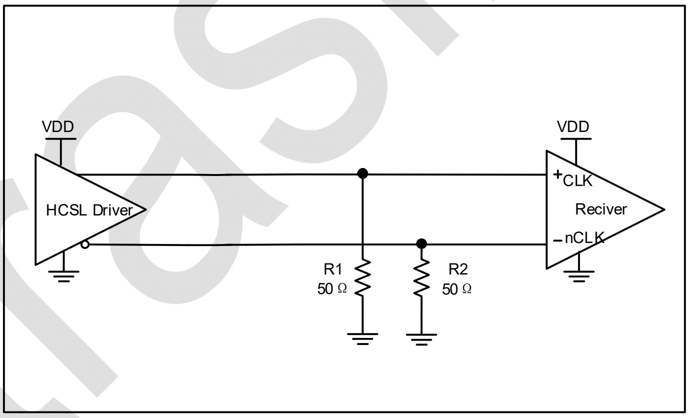
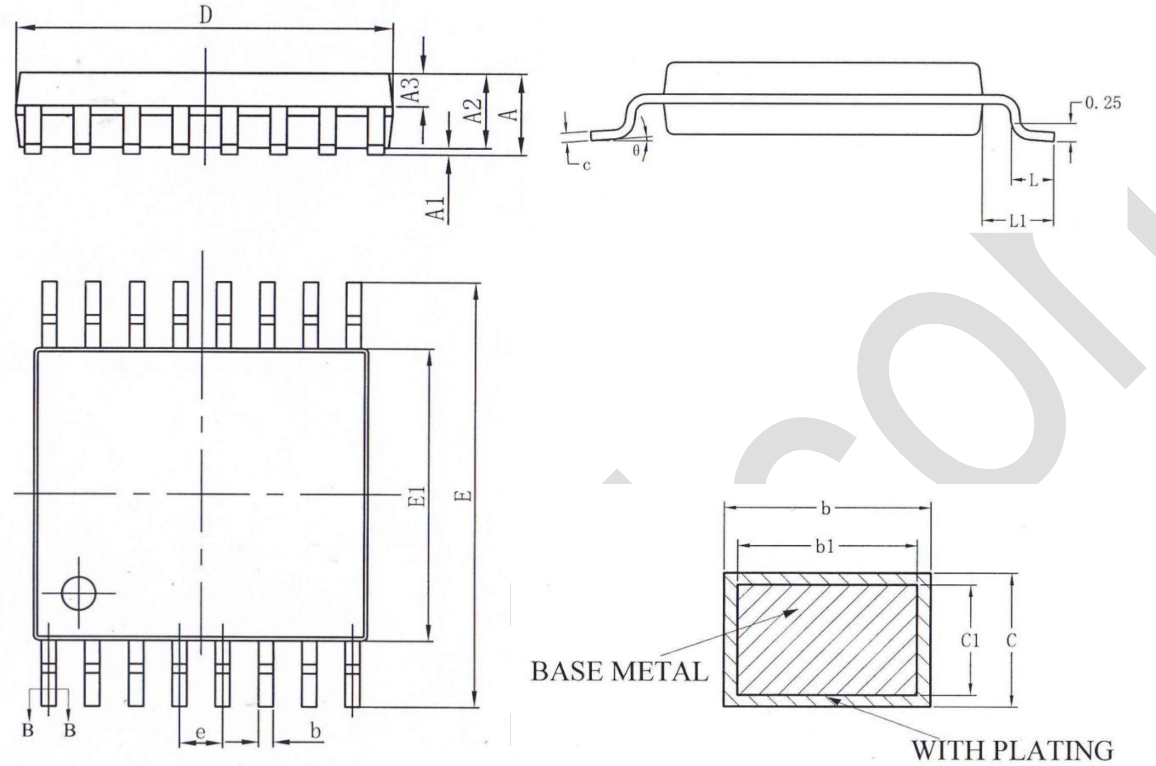


Figure5.HCSL Driver

Package Outlines



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Reflow profile

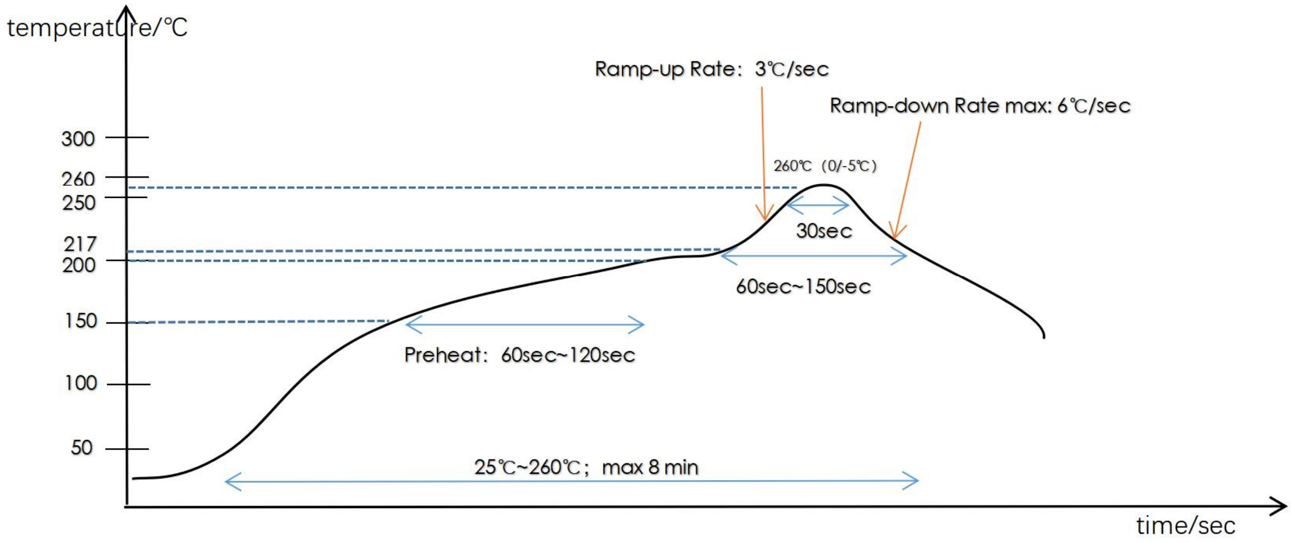


Figure6: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.01.30	First Draft.	1.0
2023.03.12	Add the test result of Phase jitter.	1.5
2026.01.23	Add product trademark.	2.0