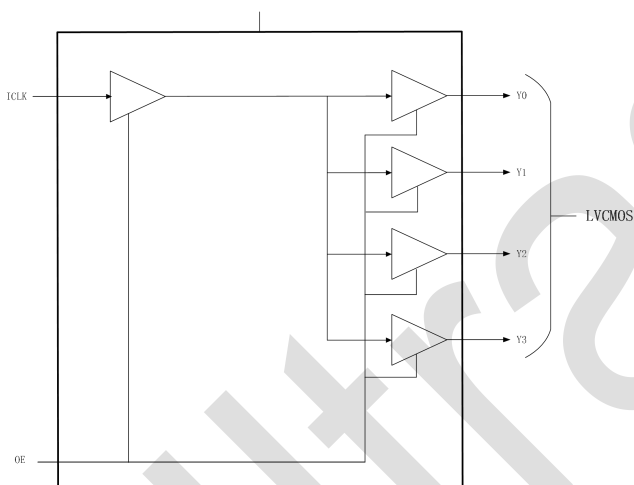


Description

The US5S104B is a low skew, single input to four output, clock buffer. Part of Ultrasilicon' Clock family, this is a low skew, small clock buffer.

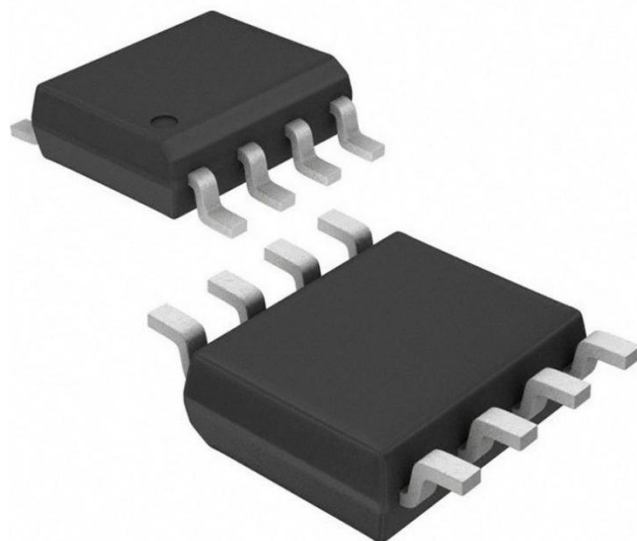
Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from -40°C to 85°C .

Block Diagram

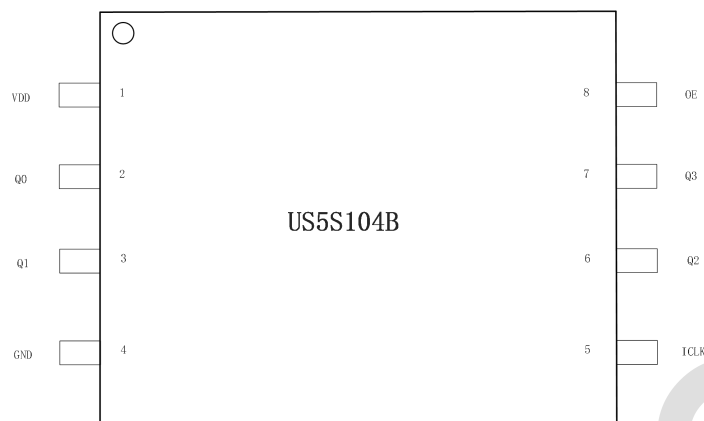


Features

- High-Performance 1:4 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 50 ps (Typical)
- Very low propagation delay < 3 ns
- Synchronous Output Enable Is Available
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range: -40°C to 85°C
- Available in 8-Pin SOP Package



Pin Assignment



Pin Descriptions and Function Table

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +1.8V, +2.5V, +3.3V
2	Q0	Output	LVC MOS Output 0, Typically connected to a receiver. Unused outputs can be left floating.
3	Q1	Output	LVC MOS Output 1, Typically connected to a receiver. Unused outputs can be left floating.
4	GND	Power	Ground
5	ICLK	Input	Clock Input. 3.3V tolerant input.
6	Q2	Output	LVC MOS Output 2, Typically connected to a receiver. Unused outputs can be left floating.
7	Q3	Output	LVC MOS Output 3, Typically connected to a receiver. Unused outputs can be left floating.
8	OE	Input	Output Enable. Tri-states outputs when low. Connect to VDD for normal operation. This pin has an 50k Ω internal pull-down resistor.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
V _{DD} : Supply voltage	4.6V
ICLK : Input voltage	-0.3V ~ VDD + 0.3V
T _J : Junction Temperature	150°C
T _{STG} : Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T _A	Ambient air temperature	-40		85	°C
T _J	Junction temperature			125	°C
V _{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	
		1.8-5%	1.8	1.8+5%	

DC Electrical Characteristics

VDD=1.8V ±5% , Ambient temperature -40°C to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, ICLK	VIL				0.3*VDD	V
Input High Current, ICLK, OE	IIH				40	uA
Input Low Current, ICLK, OE	IIL				1.5	uA
Input High Voltage, OE	VIH		0.7 x VDD		VDD	V
Input Low Voltage, OE	VIL				0.3 x VDD	V
Output High Voltage	VOH	IOH = -8 mA	1.4			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		15		mA

VDD=2.5V ±5%, Ambient temperature -40°C to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, ICLK	VIL				0.3*VDD	V
Input High Current, ICLK, OE	IIH				55	uA
Input Low Current, ICLK, OE	IIL				2	uA
Input High Voltage, OE	VIH		0.7 x VDD		VDD	V
Input Low Voltage, OE	VIL				0.3 x VDD	V
Output High Voltage	VOH	IOH = -8 mA	2			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		19		mA

VDD=3.3V ±5% , Ambient temperature -40°C to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Input High Voltage, ICLK	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, ICLK	VIL				0.3*VDD	V
Input High Current, ICLK, OE	IIH				80	uA
Input Low Current, ICLK, OE	IIL				3	uA
Input High Voltage, OE	VIH		0.7x VDD		VDD	V
Input Low Voltage, OE	VIL				0.3 x VDD	V
Output High Voltage	VOH	IOH = -8 mA	2.8			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		24		mA

AC Electrical Characteristics

VDD = 1.8V \pm 5%, Ambient Temperature -40°C to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		200	MHz
Output Rise Time	t _{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t _{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			2.0	4.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	Jitter _{ADD}	100MHz, 12KHz to 20MHz		105		fs

VDD = 2.5V \pm 5%, Ambient Temperature -40°C to +85°C, unless stated otherwise

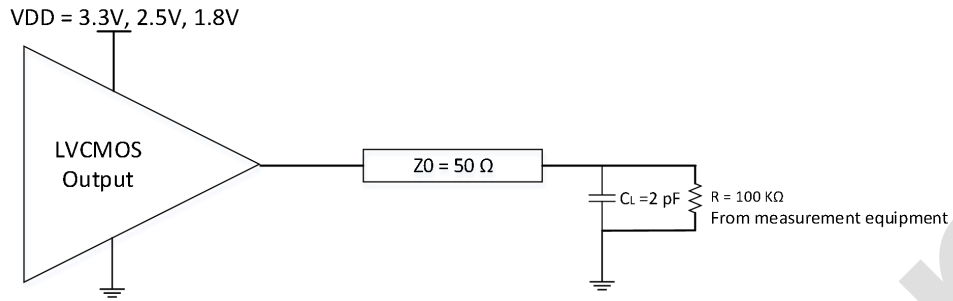
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		200	MHz
Output Rise Time	t _{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t _{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			1.5	3.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	Jitter _{ADD}	100MHz, 12KHz to 20MHz		50		fs

VDD = 3.3V \pm 5%, Ambient Temperature -40°C to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		250	MHz
Output Rise Time	t _{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t _{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			1.0	2.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	Jitter _{ADD}	100MHz, 12KHz to 20MHz		25		fs

Notes: 1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

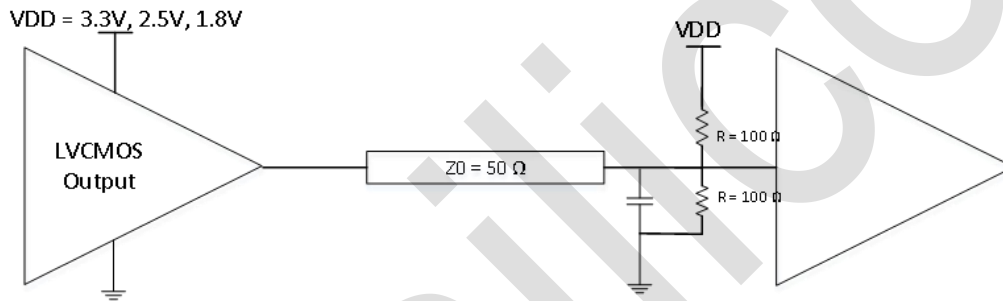
Parameter Measurement Information



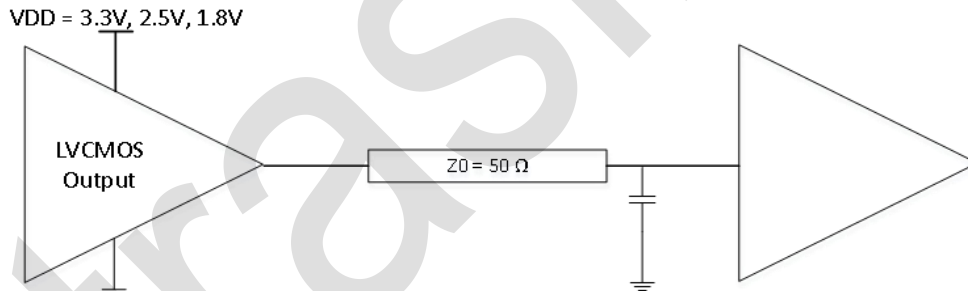
Test Load Circuit

Note:

1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency $\leq 250\text{MHz}$, $Z_0 = 50 \Omega$, $t_r < 1.2\text{ns}$, $t_f < 1.2\text{ns}$.

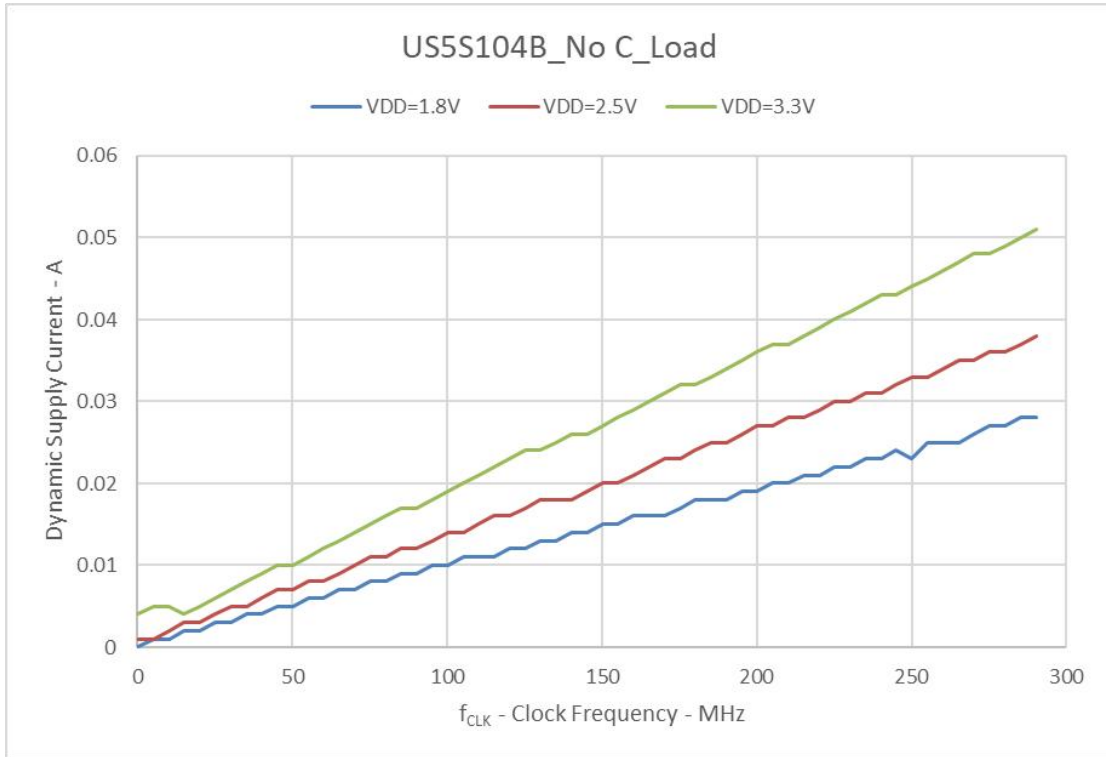


Application Load Witch 50-Ω Termination

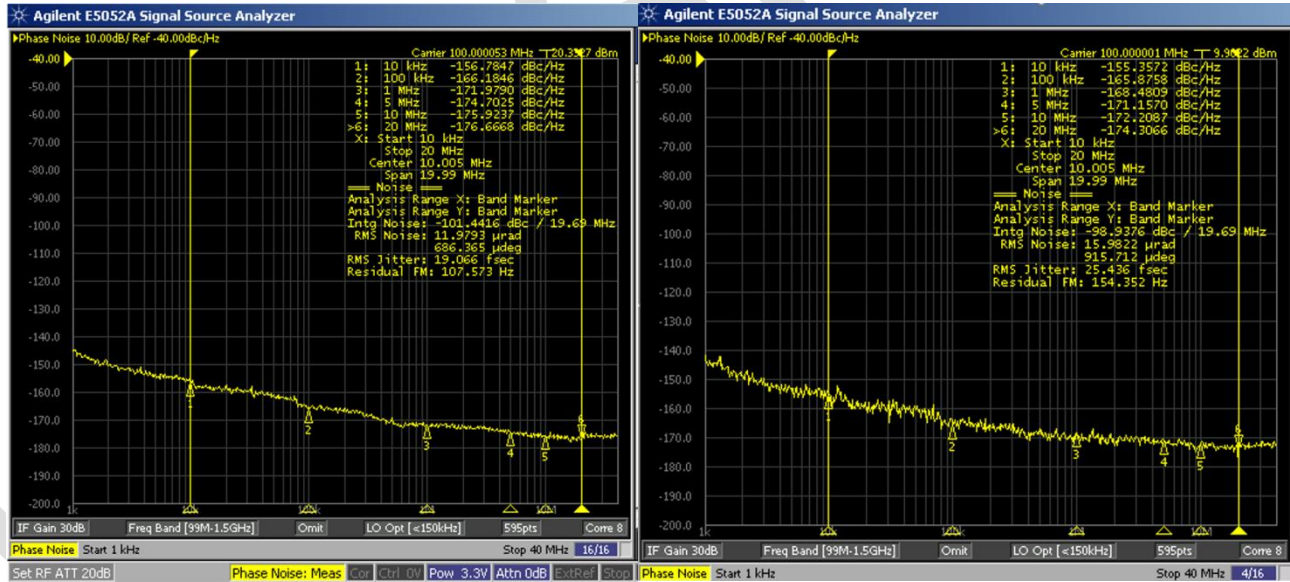


Application Load With Termination

Dynamic Supply Current vs. Clock Frequency



Phase Noise Plot

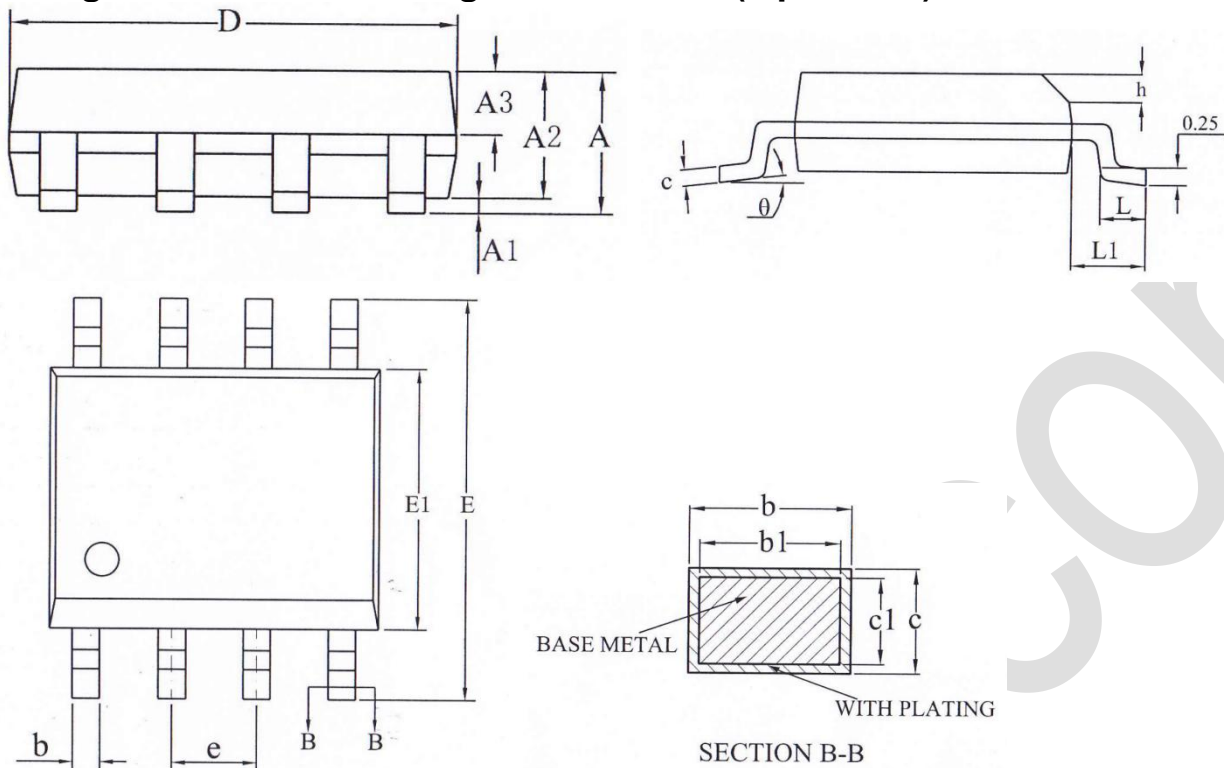


Wenzel 100MHz OCXO(19fs)

Output Phase Noise(25.5fs)

The additive phase jitter for this device was measured using the Wenzel 100MHz OCXO(19fs) as an input source with an Agilent E5052A phase noise analyzer. (VDD=3.3V)

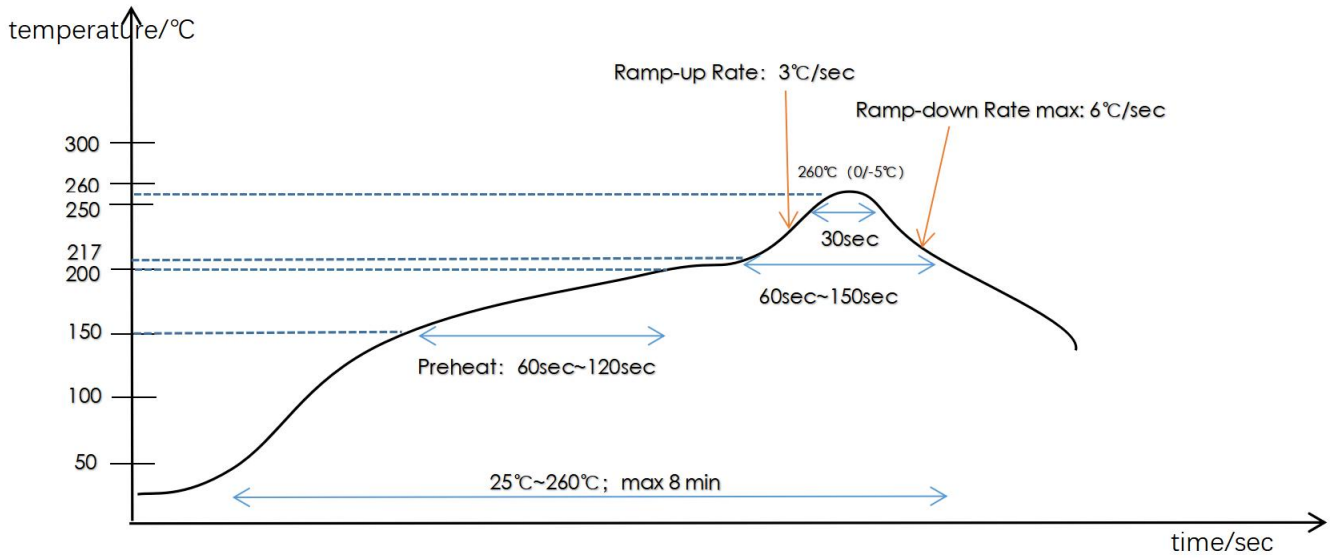
Package Outline and Package Dimensions (8 pin SOP)



Package dimensions are kept current with JEDEC Publication No. 95

Symbol	Millimeters		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 Basic		
h	0.25	-	0.50
L	0.50	-	0.80
θ	0°	-	8°

Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0
2023.02.10	Operating frequency range change.	1.5

Ultrasilicon