4-LVDS Output Ultra-Low Additive Jitter/Differential Clock Buffer

Description

The US5D2102D is a 2-GHz,4-output differential high-performance clock fanout buffer.

The US5D2102D clock buffer distributes one of two selectable clock inputs to four pairs of differential LVDS clock outputs (Q0, Q3) with minimum skew for clock distribution. Each buffer block consists of one input and two LVDS clock outputs. The Inputs inputs can be LVPECL, LVDS, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0)
- Remote Radio Units and Baseband Units

Features

- 2:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS and LVCMOS
- Four LVDS output
- Maximum Output Frequency
  LVPECL - 2-GHz
- Maximum Propagation Delay: 450 ps(typical)
- Output skew: 20 ps (typical)
- Part-to-part skew: 100ps
- Additive RMS phase jitter @ 156.25MHz:
  300fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage mode: VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-16 3x3 package

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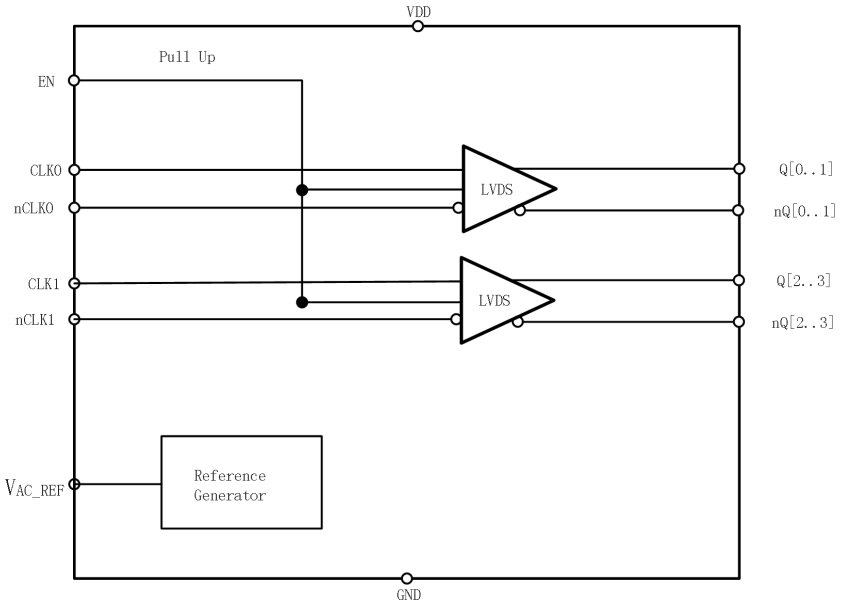
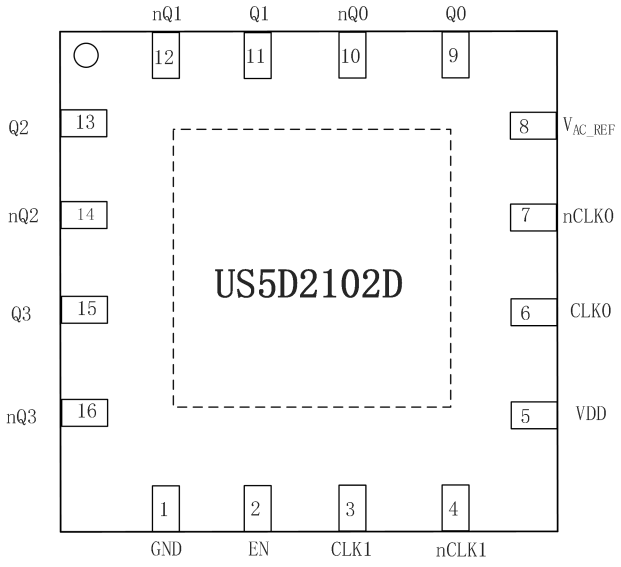
Block Diagram



Pin Assignment for QFN-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
2	EN	Input	Control pin – enables or disables the outputs.(See Table 2.)
3	CLK1	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
4	nCLK1	Input	Inverting differential input pair .Unused input pair can be left floating.
5	VDD	Power	2.5V or 3.3-V supply for the device.
6	CLK0	Input	Differential input pair or single-ended input. Unused input pair can be left floating
7	nCLK0	Input	Inverting differential input pair .Unused input pair can be left floating.
8	VAC_REF	Output	Bias voltage output for capacitive-coupled inputs. Do not use VAC_REF at VDD < 3 V. If used, it is recommended to use a 0.1- μ F capacitor to GND on this pin.
9	Q0	Output	Differential LVDS output pair no. 0. Unused output pair can be left floating
10	nQ0	Output	Differential LVDS output pair no. 0. Unused output pair can be left floating
11	Q1	Output	Differential LVDS output pair no. 1. Unused output pair can be left floating
12	nQ1	Output	Differential LVDS output pair no. 1. Unused output pair can be left floating
13	Q2	Output	Differential LVDS output pair no. 2. Unused output pair can be left floating
14	nQ2	Output	Differential LVDS output pair no. 2. Unused output pair can be left floating
15	Q3	Output	Differential LVDS output pair no. 3. Unused output pair can be left floating
16	nQ3	Output	Differential LVDS output pair no. 3. Unused output pair can be left floating

Table 2: Output Control Table

EN	CLOOCK OUTPUTS
0	All outputs disabled
OPEN	All outputs enabled
1	Q0,Q1 enabled andQ2, Q3 disabled

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±3000	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±200	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics(INPUT)

At VCC = 2.375 V to 3.6 V and TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVCMOS input						
FIN	Input Frequency	VDD=3.3V	0.1		250	MHz
Vth	Input threshold voltage	External threshold voltage applied to complementary input.	1.1		1.8	V
VIH	Input high voltage		1.2		VDD	V
VIL	Input low voltage		0		1.7	V
IIH	Input high current	VDD = 3.6 V, VIH = 3.6 V			-40	μA
IIL	Input low current	VDD = 3.6 V, VIL = 0 V			-40	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
C_{IN}	Input capacitance			5		pF
Differential Input						
FIN	Input frequency	VDD=3.3V	0.1		2000	MHz
$V_{IN,DIFF,PP}$	Differential input peal-peak voltage	FIN ≤ 1.5 GHz	0.1		1.5	V
		1.5 GHz ≤ FIN ≤ 2 GHz	0.2		1.5	V
VICM	Input common-mode level		1		VDD-0.3	V
IIH	Input high current	VDD = 3.6 V, VIH = 3.6 V			-40	μA
IIL	Input low current	VDD = 3.6 V, VIL = 0 V			-40	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
C_{IN}	Input capacitance			5		pF

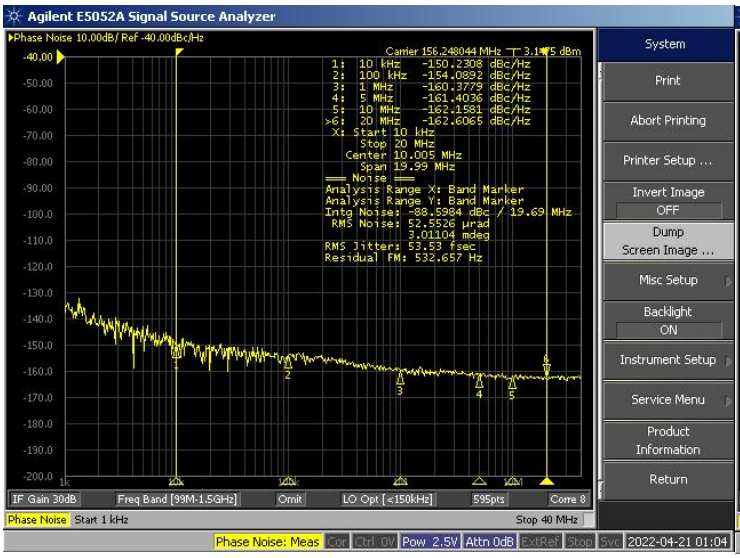
Electrical Characteristics(OUTPUT)

VDD = 3.125V to 3.6 V; TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

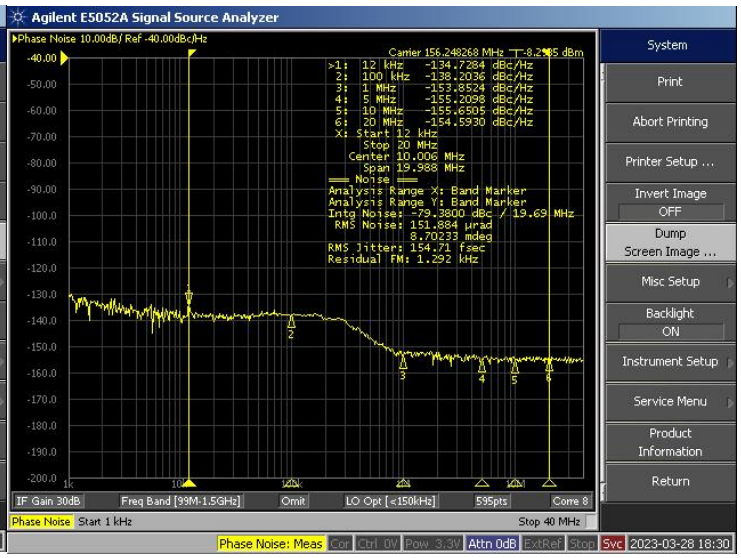
Parameter		Test Conditions	Min	Typ	Max	Unit
LVDS Output						
V_{OD}	Differential output voltage magnitude	VIN, DIFF, PP = 0.3 V,RL = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude		-15		15	mV
V_{SS}	Steady-state common mode output voltage		1.1		1.375	V
ΔV_{SS}	Change in common mode output voltage	VIN, DIFF, PP = 0.6 V,RL = 100 Ω	-15		15	mV
Vring	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
VOH	Ouput high voltage		VDD-1.2		VDD-0.9	V
VOL	Output low voltage		VDD-1.7		VDD-1.3	V
Ios	Short-circuit output current	V_{OD}=0V			±24	mA
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{load} = 100 µA	1.1	1.25	1.35	V
t_{PD}	Propagation delay				450	ps
$t_{SK,PP}$	Part-to-part skew				100	ps
$t_{SK,O}$	Output skew				20	ps
$T_{sk,p}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, F_{OUT}=100MHz	-50		50	ps
t_{RJIT}		Additive RMS phase jitter @ 100MHz: (10kHz - 20MHz)			300	fs rms
t_R/t_F	Output rise/fall time	20% to 80%			200	ps
I_{cc100}	Supply current	All outputs enabled, R_L=100Ω, f=100MHz		49	77	mA
I_{cc800}	Supply current	All outputs enabled, R_L=100Ω, f=800MHz		76	106	

Tip:Internally generated bias voltage (VAC_REF) is for 3.3 V operation only. It is recommended to apply externally generated bias voltage for VDD< 3 V.

Phase Noise Plot



Low jitter SPXO(156.25MHz)(53fs)



Output Phase Noise(154fs)

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

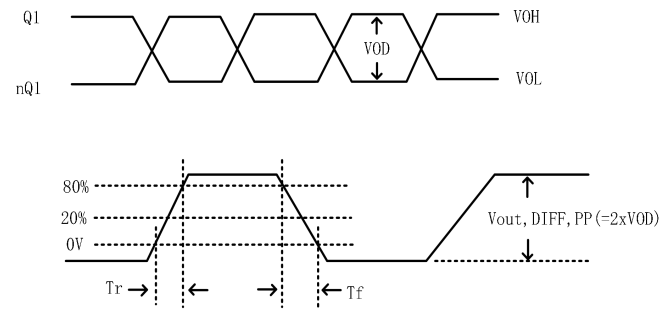
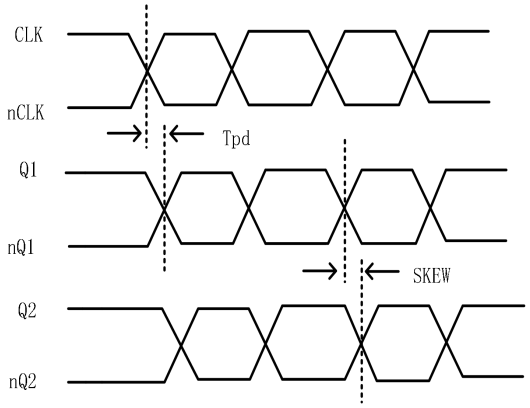


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2,3), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2,3).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2,3) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2,3) across multiple devices

Figure 2.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

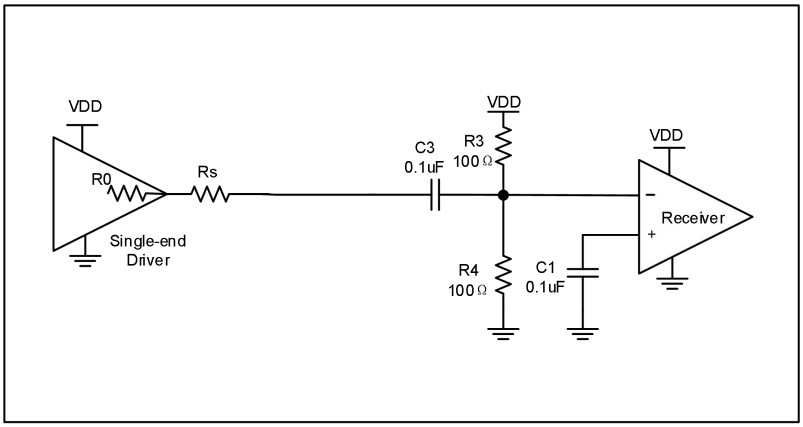
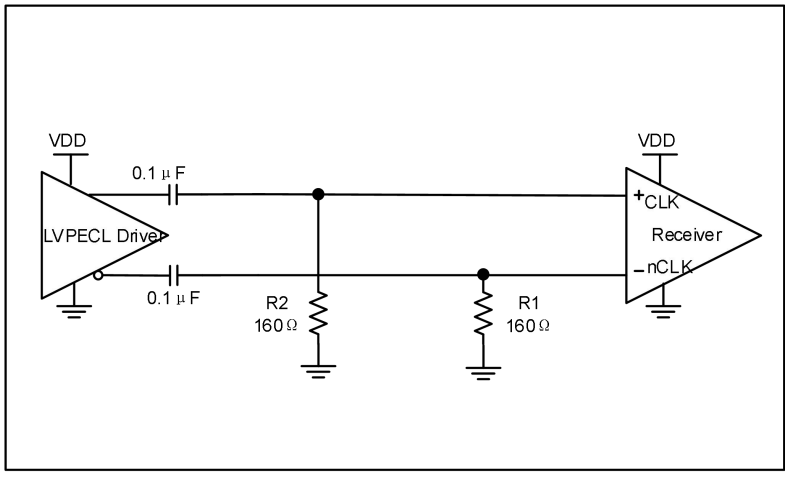
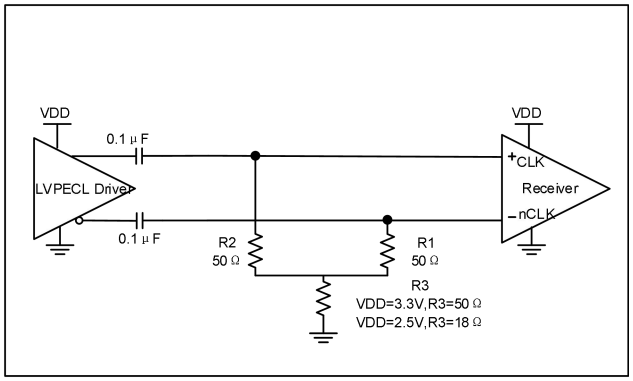


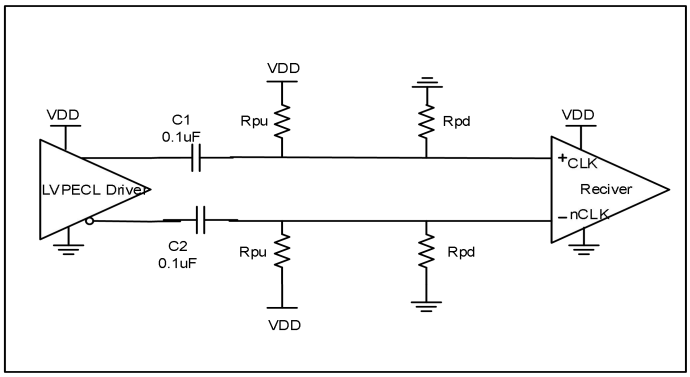
Figure3.Single-ended input

Input connection circuit

The CLK/nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure4 to Figure8 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

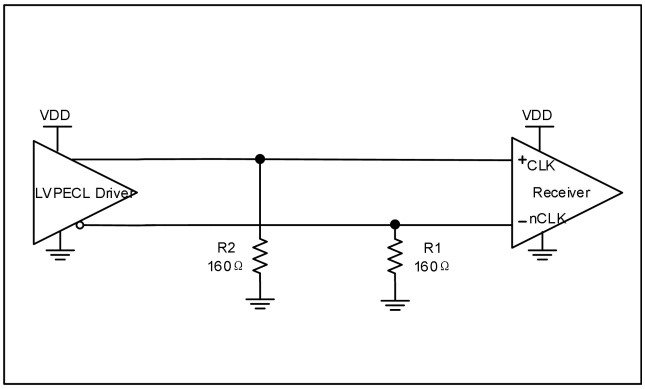


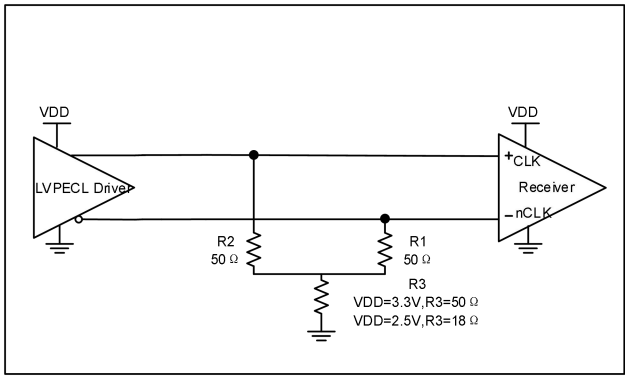


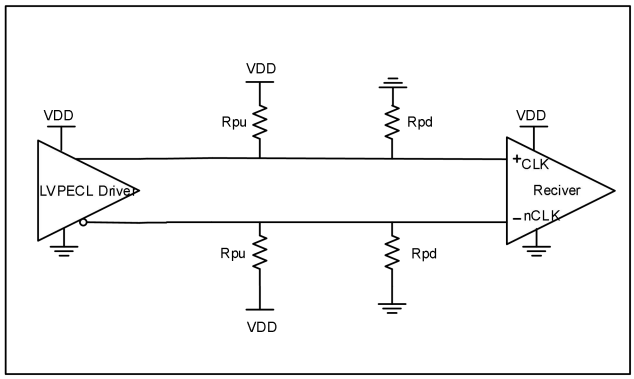


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure4.LVPECL Driver(AC)

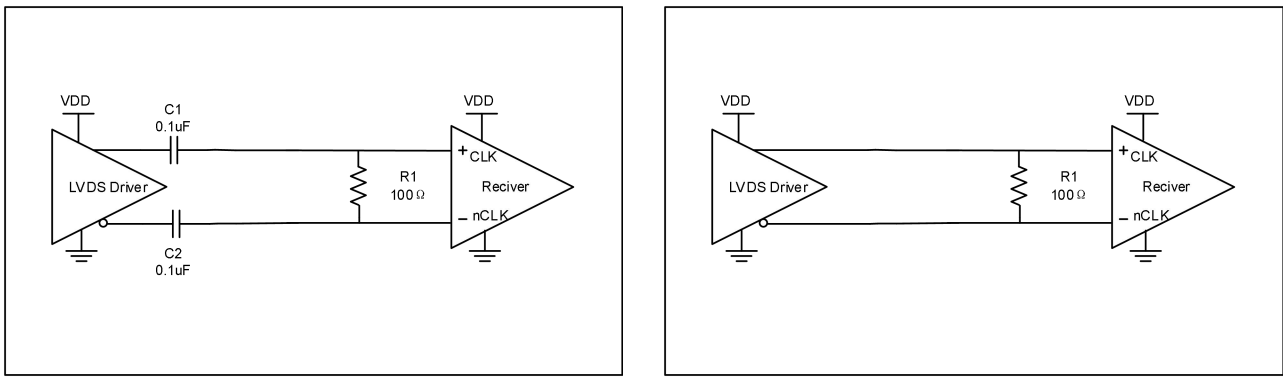






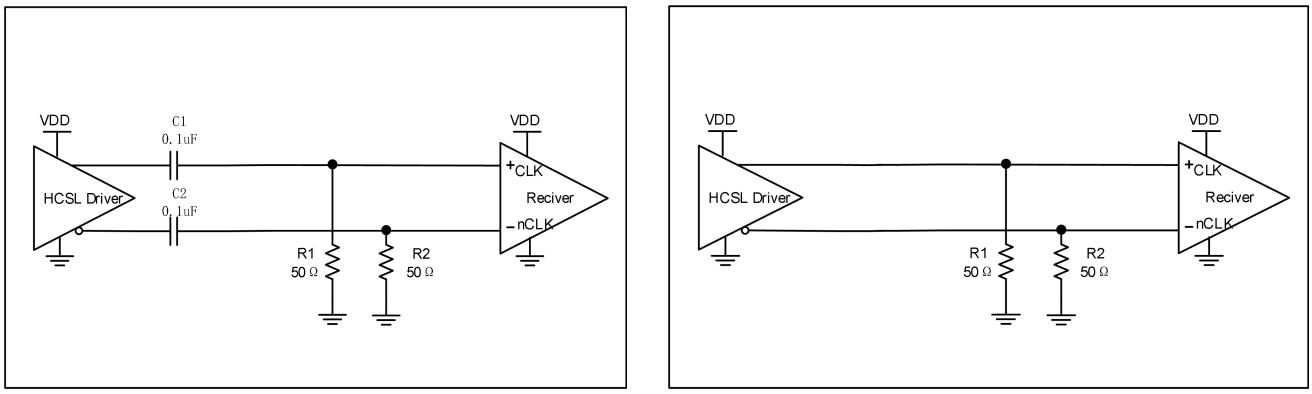
VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

Figure6.LVDS Driver



a)AC coupling **b)DC coupling**

Figure7.HCSL Driver

Output connection circuit

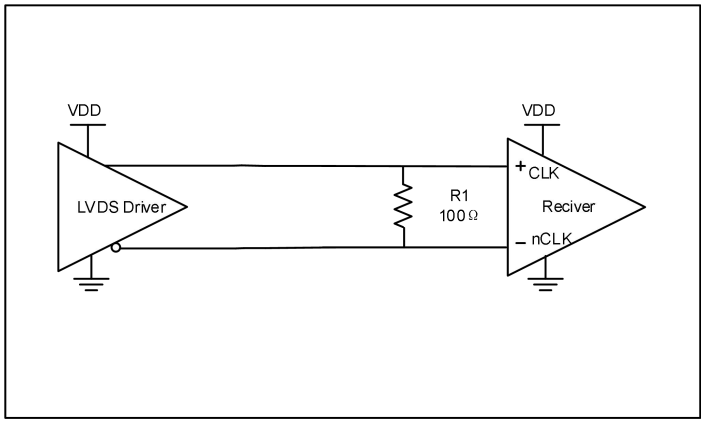
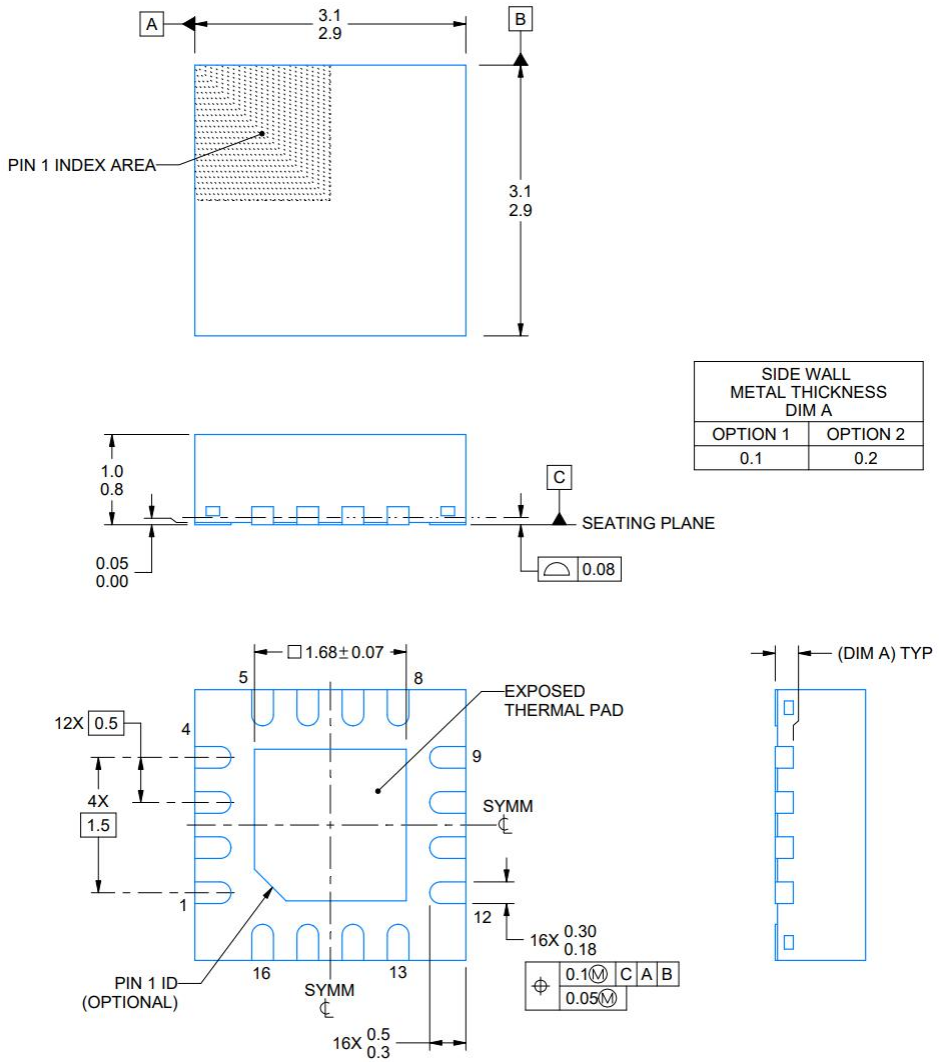


Figure8.LVDS Driver

PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

Reflow profile

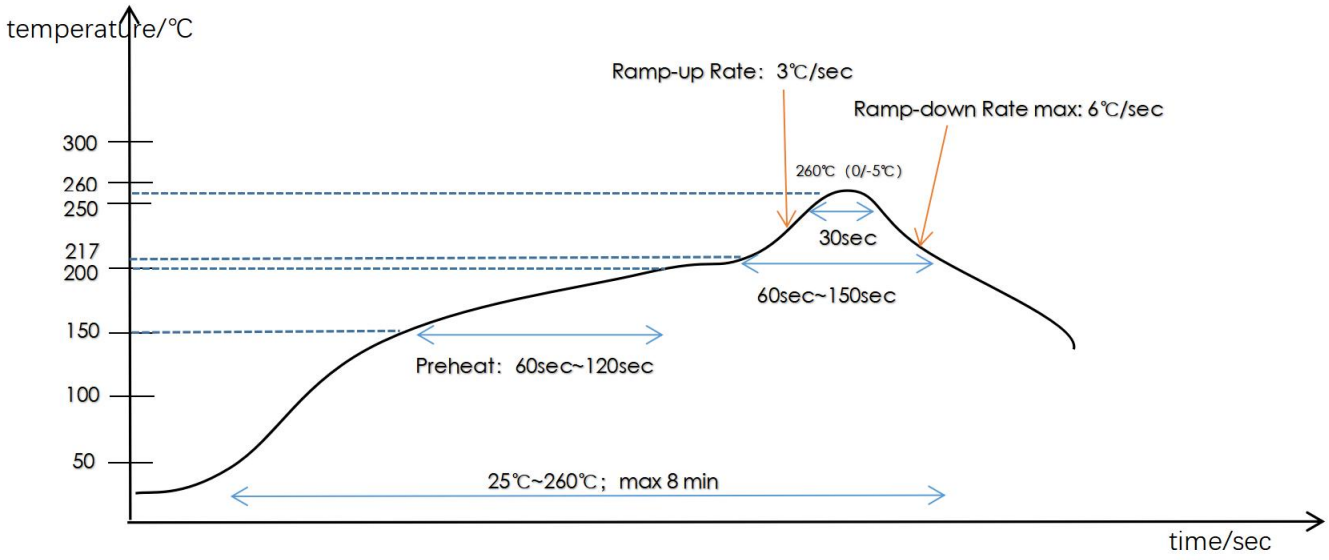


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.4.18	First Draft.	1.0
2023.5.11	Update Update Timing Diagrams and input selecton.	1.5
2023.12.05	Modify the LVCMOS input connection	2.0