

## Description

The US5D2102P is a 2-GHz,4-output differential high-performance clock fanout buffer.

The US5D2102P clock buffer distributes one of two selectable clock inputs to four pairs of differential LVPECL clock outputs (Q0~ Q3) with minimum skew for clock distribution. Each buffer block consists of one input that feeds two LVPECL clock outputs. The Inputs inputs can be LVPECL, LVDS, or LVCMOS/LVTTL. It has a maximum clock frequency up to 2-GHz.

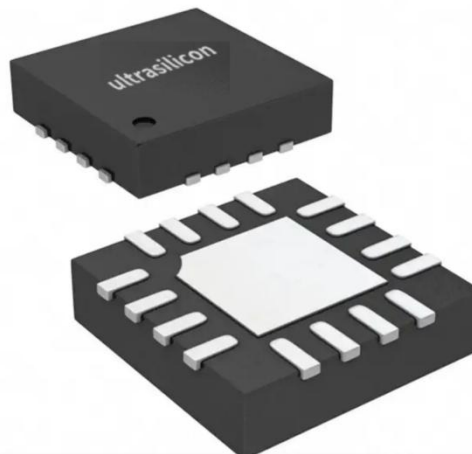
The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

## Applications

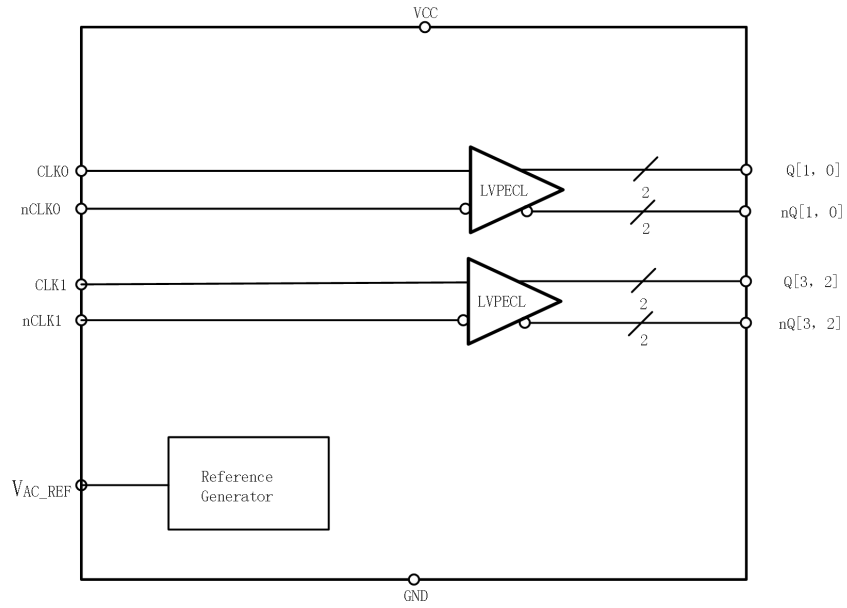
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0)
- Remote Radio Units and Baseband Units

## Features

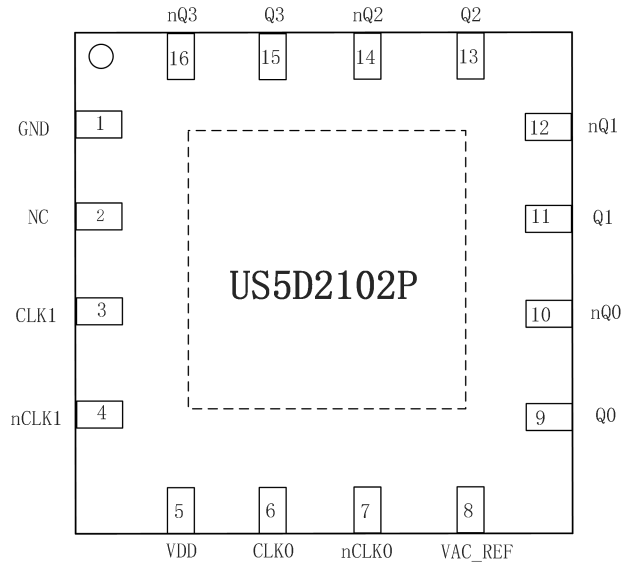
- 2:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS and LVCMOS/LVTTL
- Four LVPECL output
- Maximum Output Frequency  
LVPECL - 2-GHz
- Maximum Propagation Delay: **450 ps**(typical)
- Output skew: **20 ps** (typical)
- Part-to-part skew: **100ps**
- Additive RMS phase jitter @ 156.25MHz:  
**48fs RMS** (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage mode: VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-16 package



## Block Diagram



## Pin Assignment for QFN-16 Package



## Pin Description and Pin Characteristic Tables

**Table 1: Pin Descriptions**

Number	Name	Type	Description
1	GND	Power	Ground.
2	NC	-	Do not connect.
3	CLK1	Input	Differential input pair. Unused input pair can be left floating.
4	nCLK1	Input	Inverting differential input pair .
5	VDD	Power	2.5V or 3.3-V supply for the device.
6	CLK0	Input	Differential input pair. Unused input pair can be left floating.
7	nCLK0	Input	Inverting differential input pair . Unused input pair can be left floating.
8	VAC_REF	Output	Bias voltage output for capacitive-coupled inputs. Do not use VAC_REF at VCC < 3 V. If used, it is recommended to use a 0.1- $\mu$ F capacitor to GND on this pin. The output current is limited to 2 mA.
9	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating
10	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating
11	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating
12	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating
13	Q2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating
14	nQ2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating
15	Q3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating
16	nQ3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating

**Table 2: Input Selection Table**

IN_SEL	ACTIVE CLOCK INPUT
0	CLK0,nCLK0
1	CLK1,nCLK1

## Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
V <sub>DD</sub>	4.6V
V <sub>IN</sub>	-0.5V to V <sub>DD</sub> + 0.5V
T <sub>J</sub> :Junction Temperature	125°C
T <sub>STG</sub> :Storage Temperature	-65°C to 150°C

## ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±3000	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±200	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

## Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>A</sub>	Ambient air temperature	-40		85	°C
T <sub>J</sub>	Junction temperature			125	°C
V <sub>DD</sub>	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

## Electrical Characteristics(INPUT)

At VCC = 2.375 V to 3.6 V and TA = -40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>LVC MOS input</b>						
FIN	Input Frequency	VDD=3.3V	0.1		250	MHz
Vth	Input threshold voltage	External threshold voltage applied to complementary input.	1.1		1.8	V
VIH	Input high voltage		1.2		VDD	V
VIL	Input low voltage		0		1.7	V
IIH	Input high current	VCC = 3.6 V, VIH = 3.6 V			-40	μA
IIL	Input low current	VCC = 3.6 V, VIL = 0 V			-40	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
CIN	Input capacitance			5		pF
<b>Differential Input</b>						
FIN	Input frequency	VDD=3.3V	0.1		2000	MHz
VIN,DIFF,PP	Differential input peak-peak voltage	FIN ≤ 1.5 GHz	0.1		1.5	V
		1.5 GHz ≤ FIN ≤ 2 GHz	0.2		1.5	V
VICM	Input common-mode level		1		VDD-0.3	V
IIH	Input high current	VCC = 3.6 V, VIH = 3.6 V			-40	μA
IIL	Input low current	VCC = 3.6 V, VIL = 0 V			-40	μA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
CIN	Input capacitance			5		pF

## Electrical Characteristics(OUTPUT)

VCC = 2.375 V to 2.625 V; TA = -40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

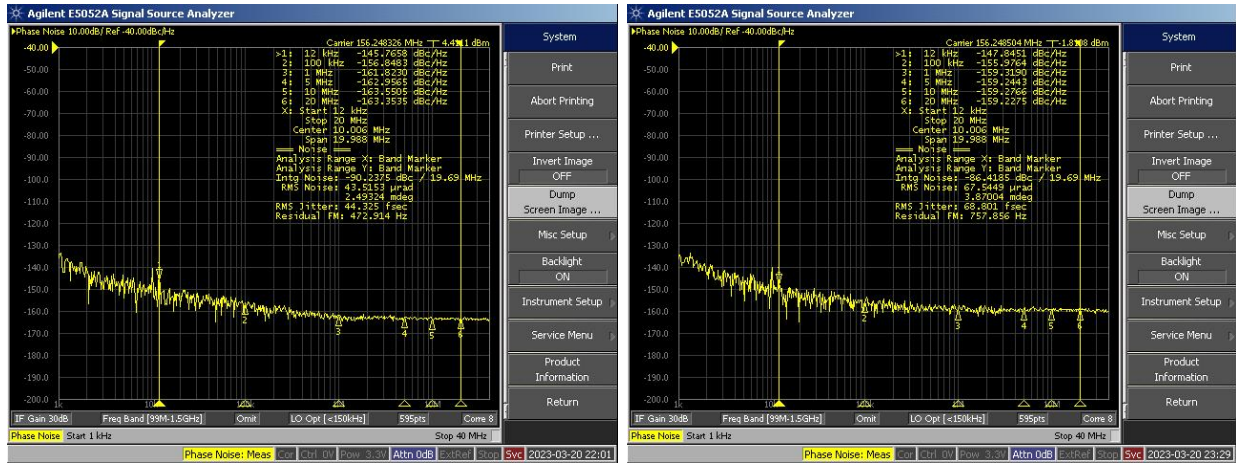
Parameter		Test Conditions	Min	Typ	Max	Unit
<b>LVPECL Output</b>						
VOH	Output high voltage		V <sub>DD</sub> -1.2		V <sub>DD</sub> -0.9	V
VOL	Output low voltage		V <sub>DD</sub> -1.7		V <sub>DD</sub> -1.3	V
VOUT,DIFF,PP	Differential output peak-peak voltage	f <sub>IN</sub> ≤ 2 GHz	0.5		1.35	V
V <sub>AC_REF</sub>	Input bias voltage	I <sub>AC_REF</sub> = 2 mA	V <sub>DD</sub> -1.6		V <sub>DD</sub> -1.1	V
t <sub>PD</sub>	Propagation delay				450	ps
t <sub>SK,PP</sub>	Part-to-part skew				100	ps
t <sub>SK,O</sub>	Output skew				20	ps
T <sub>sk,p</sub>	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, F <sub>OUT</sub> =100MHz	-50		50	ps
t <sub>RJIT</sub>		Additive RMS phase jitter @ 100MHz: (10kHz - 20MHz)		48		fs
t <sub>R</sub> /t <sub>F</sub>	Output rise/fall time	20% to 80%			200	ps

Tip: Internally generated bias voltage (V<sub>AC\_REF</sub>) is for 3.3 V operation only. It is recommended to apply externally generated bias voltage for VCC < 3 V.

VCC = 3 V to 3.6 V; TA = -40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>LVPECL Output</b>						
VOH	Output high voltage		V <sub>DD</sub> -1.2		V <sub>DD</sub> -0.9	V
VOL	Output low voltage		V <sub>DD</sub> -1.7		V <sub>DD</sub> -1.3	V
VOUT,DIFF,PP	Differential output peak-peak voltage	f <sub>IN</sub> ≤ 2 GHz	0.65		1.35	V
V <sub>AC_REF</sub>	Input bias voltage	I <sub>AC_REF</sub> = 2 mA	V <sub>DD</sub> -1.6		V <sub>DD</sub> -1.1	V
t <sub>PD</sub>	Propagation delay				450	ps
t <sub>SK,PP</sub>	Part-to-part skew				100	ps
t <sub>SK,O</sub>	Output skew				20	ps
T <sub>sk,p</sub>	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, F <sub>OUT</sub> =100MHz	-50		50	ps
t <sub>RJIT</sub>		Additive RMS phase jitter @ 100MHz: (10kHz - 20MHz)		48		fs
t <sub>R</sub> /t <sub>F</sub>	Output rise/fall time	20% to 80%			200	ps

# PHASE JITTER



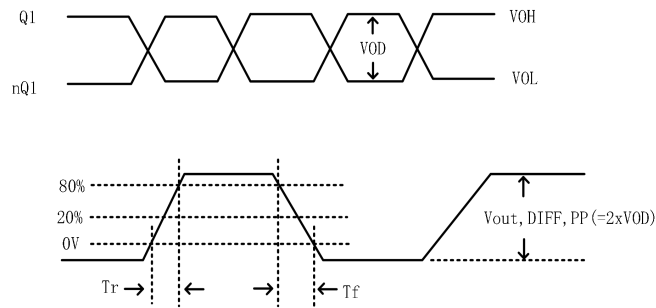
(a) Jitter\_Source

(b) 3V3\_156M25\_LVDS

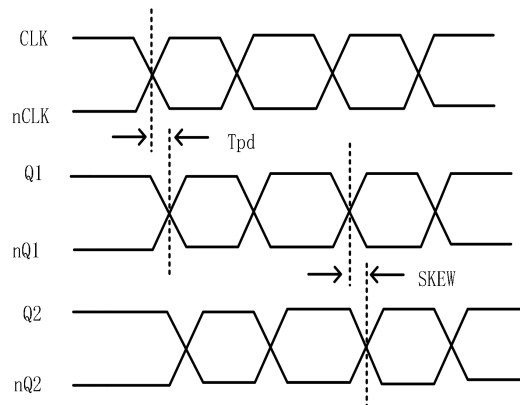
Figure 1 .RMS\_Jitter\_3V3=√(68²-44²)=51fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

## Timing Diagrams



**Figure 2.output voltage and rise/fall time**



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2,3), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2,3).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2,3) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2,3) across multiple devices

**Figure 3.output and part-to-part skew**



## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal,  $R_s$  and  $R_0$  in the driver form a  $50\ \Omega$  impedance match, and the direct-isolated capacitor  $C_3$  avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to  $V_{DD}/2$ .

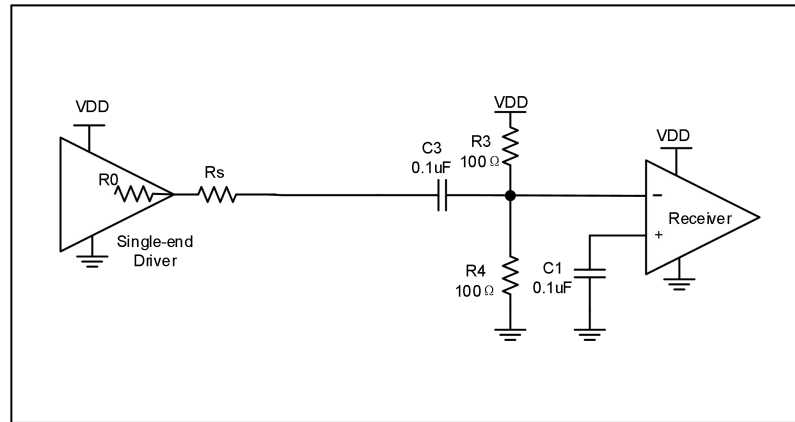
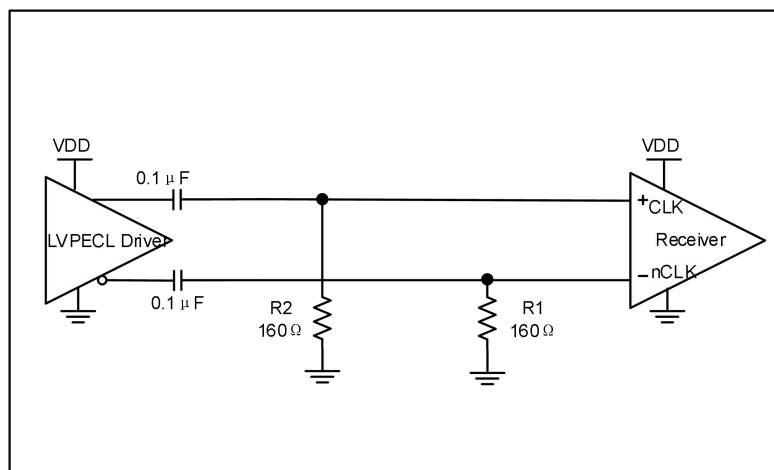
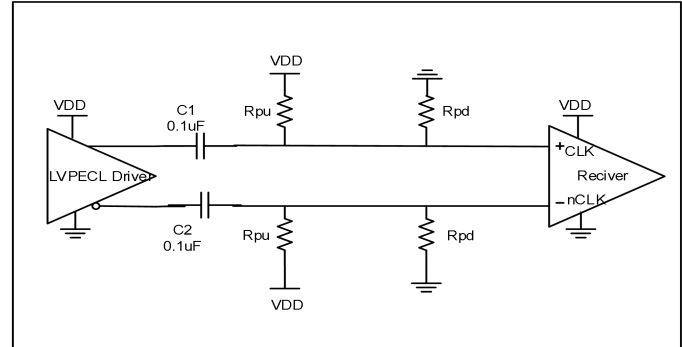
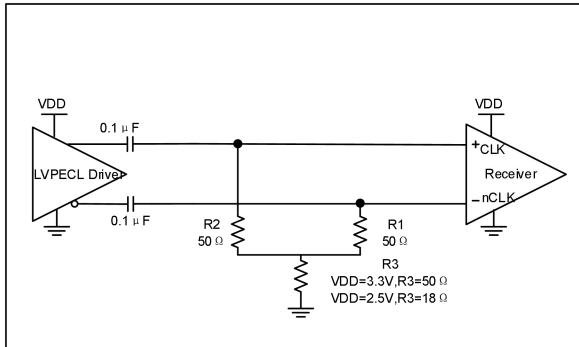


Figure4.Single-termination method of differential input

### Input connection circuit

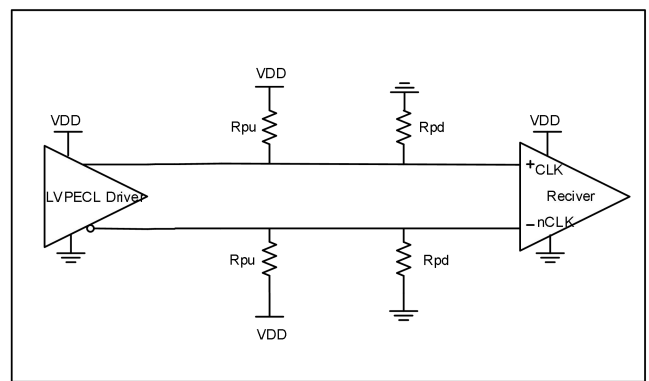
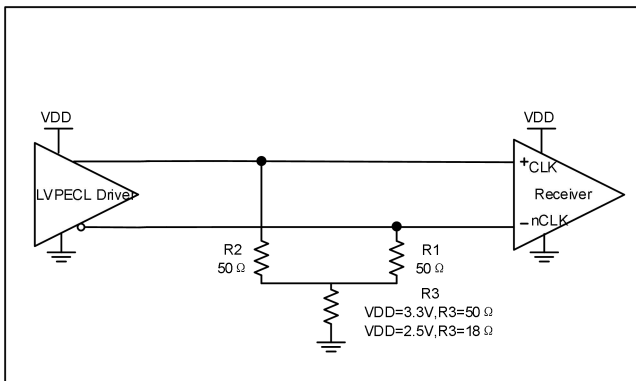
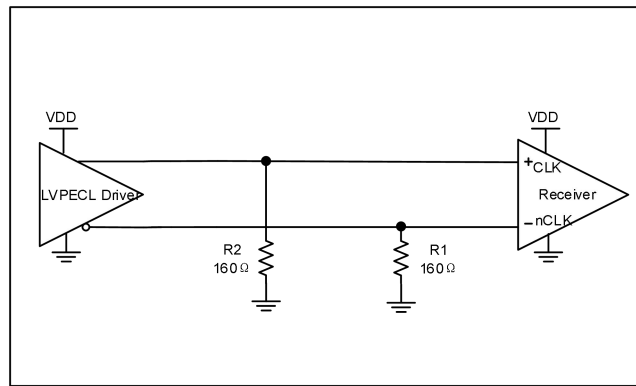
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figure5 to Figure9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.





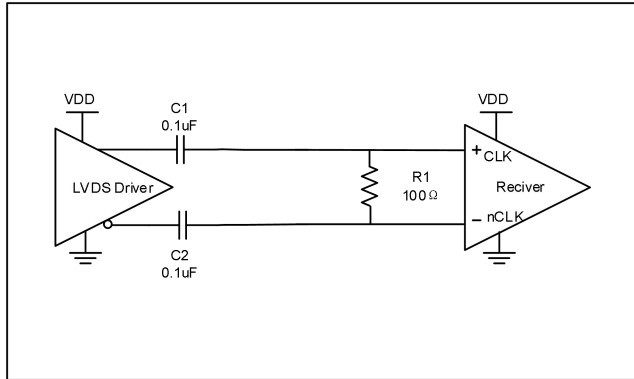
VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(AC)

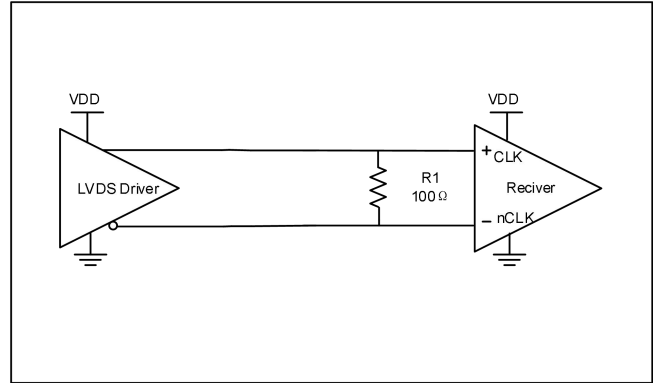


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure6.LVPECL Driver(DC)

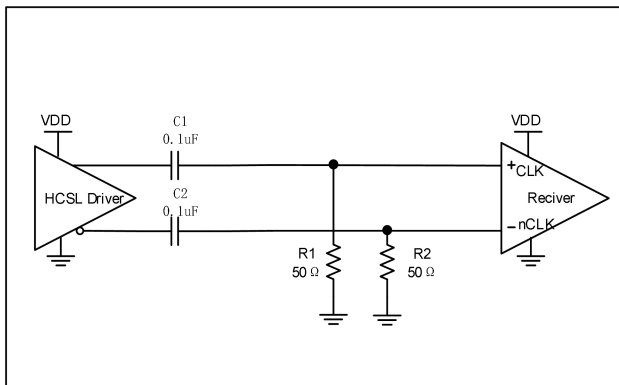


a)AC coupling

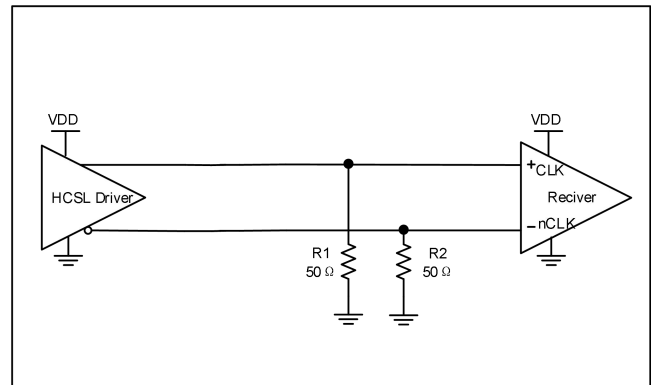


b)DC coupling

Figure7.LVDS Driver



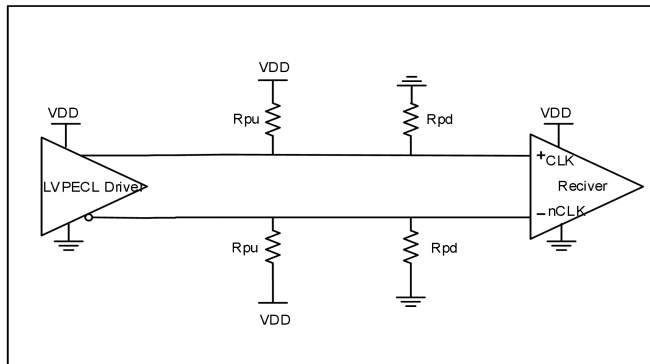
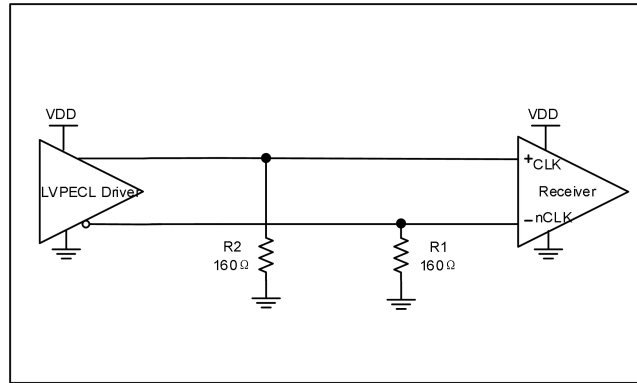
a)AC coupling



b)DC coupling

Figure8.HCSL Driver

## Output connection circuit



VDD	Rpu	Rpd
3.3V	120 $\Omega$	82 $\Omega$
2.5V	250 $\Omega$	62.5 $\Omega$

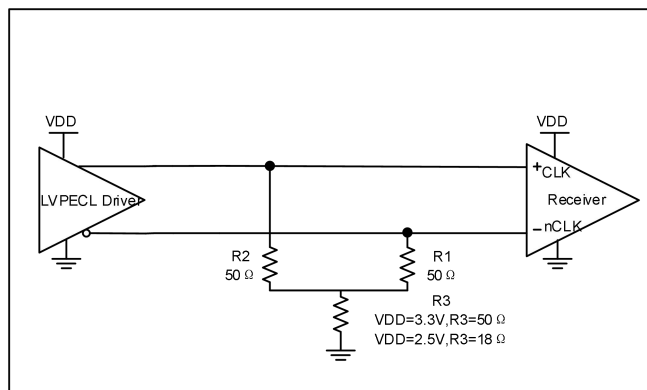
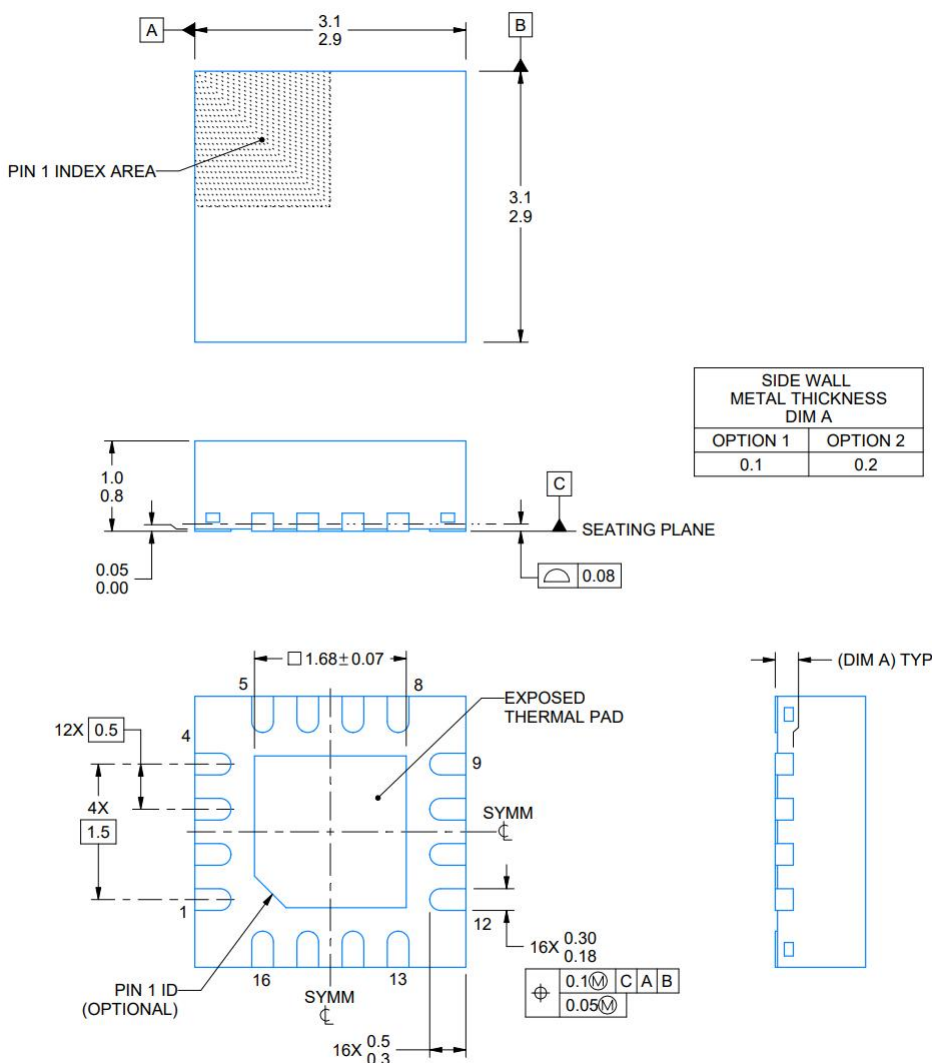


Figure9.LVPECL Driver

# PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

## Reflow profile

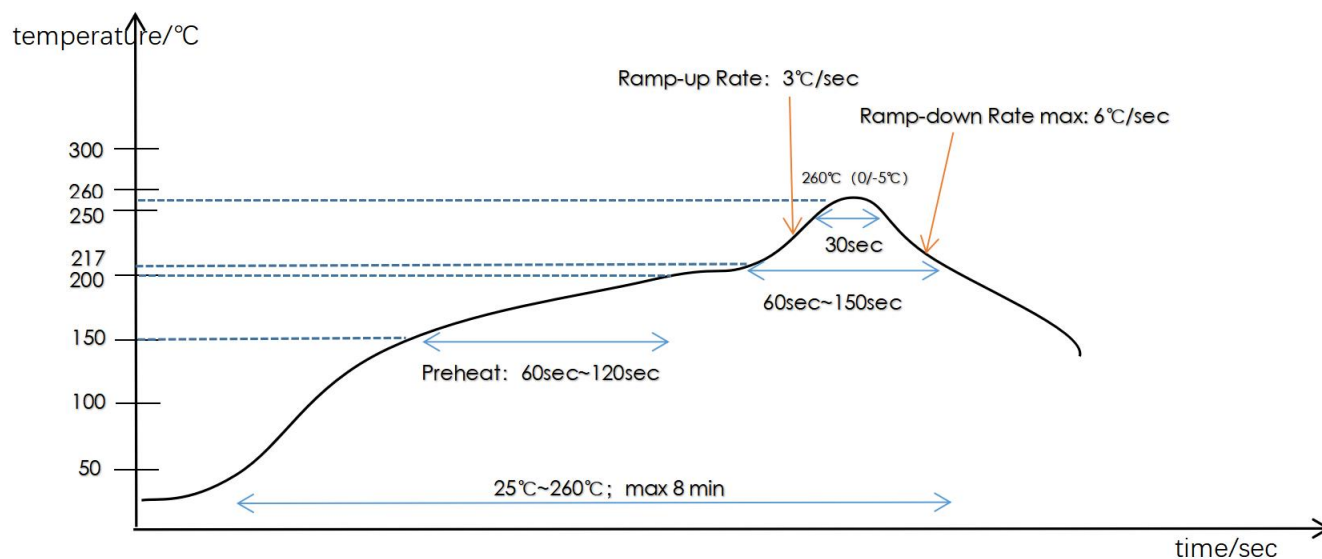


Figure26: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

## Revision History

Date	Description of Change	Revision
2022.3.1	First Draft.	1.0
2023.5.11	Update Timing Diagrams and input selecton.	1.5
2023.12.05	Modify the LVCMOS input connection	2.0