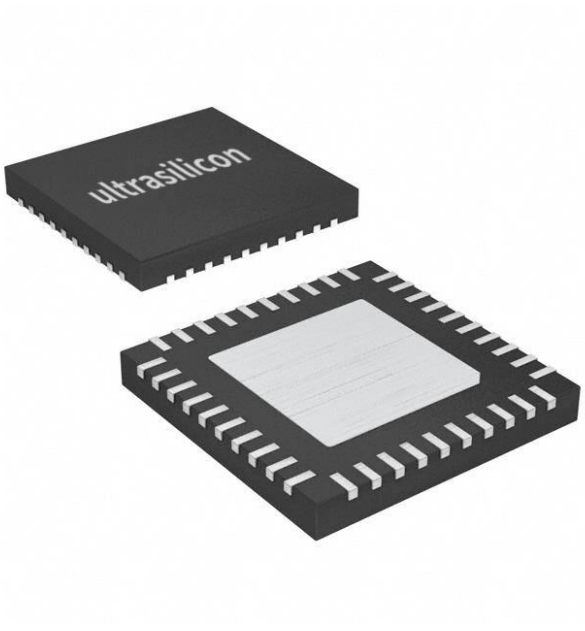
12-LVPECL Output Ultra-Low Additive Jitter/Differential Clock Buffer

US5D8954
Datasheet

Description

The US5D8954 is a 2-GHz,12-output differential high-performance clock fanout buffer.
The US5D8954 is a highly versatile, low additive jitter buffer that can generate eight copies of LVPECL clock outputs from one of two selectable LVPECL,HCSL and LVDS, or LVCMOS inputs for a variety of communication applications.It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.



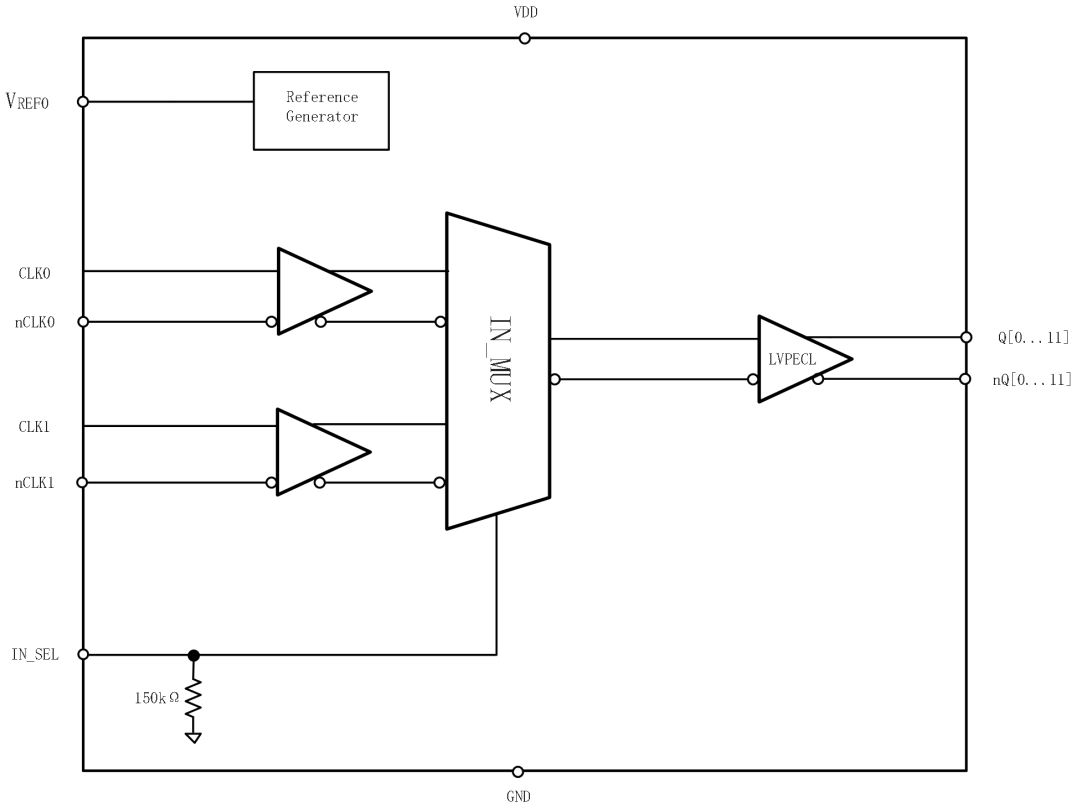
Features

- 2:12 Differential Buffer
- Universal Input Accept LVPECL,LVDS and HCSL
- Twelve LVPECL output
- Maximum Output Frequency LVPECL - 2-GHz
- Maximum Propagation Delay:500 ps(typical)
- Output skew: 20 ps (typical)
- Part-to-part skew< 500ps
- Additive RMS phase jitter @ 156.25MHz: 81fs RMS (12kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage : VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-40 package

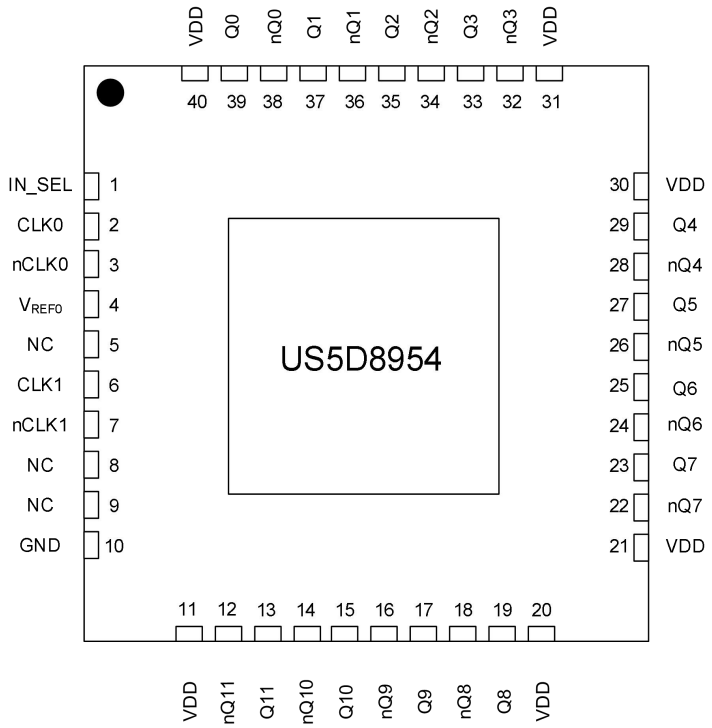
Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram



Pin Assignment for QFN-40 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	IN_SEL	Input	Input Select. Logic 0 selects CLK0 and CLK0 inputs. Logic 1 selects CLK1 and CLK1 inputs.
2	CLK0	Input	Differential input pair.
3	nCLK0	Input	Differential input pair.
4	V_{REF0}	Input	Reference Voltage. This pin provides the reference voltage for biasing ac-coupled CLK0 and nCLK0 inputs.
5	NC	---	Not connected.
6	CLK1	Input	Differential input pair.
7	nCLK1	Input	Differential input pair.
8	NC	---	Not connected.
9	NC	---	Not connected.
10	GND	Power	Ground.
11	VDD	Power	Power supply.
12	nQ11	Output	Differential LVPECL output pair no. 11. Unused output pair can be left floating.
13	Q11	Output	Differential LVPECL output pair no. 11. Unused output pair can be left floating.
14	nQ10	Output	Differential LVPECL output pair no. 10. Unused output pair can be left floating.
15	Q10	Output	Differential LVPECL output pair no. 10. Unused output pair can be left floating.
16	nQ9	Output	Differential LVPECL output pair no. 9. Unused output pair can be left floating.
17	Q9	Output	Differential LVPECL output pair no. 9. Unused output pair can be left floating.
18	nQ8	Output	Differential LVPECL output pair no. 8. Unused output pair can be left floating.
19	Q8	Output	Differential LVPECL output pair no. 8. Unused output pair can be left floating.
20	VDD	Power	Power supply.
21	VDD	Power	Power supply.
22	nQ7	Output	Differential LVPECL output pair no. 7. Unused output pair can be left floating.
23	Q7	Output	Differential LVPECL output pair no. 7. Unused output pair can be left floating.
24	nQ6	Output	Differential LVPECL output pair no. 6. Unused output pair can be left floating.
25	Q6	Output	Differential LVPECL output pair no. 6. Unused output pair can be left floating.
26	nQ5	Output	Differential LVPECL output pair no. 5. Unused output pair can be left floating.
27	Q5	Output	Differential LVPECL output pair no. 5. Unused output pair can be left floating.
28	nQ4	Output	Differential LVPECL output pair no. 4. Unused output pair can be left floating.
29	Q4	Output	Differential LVPECL output pair no. 4. Unused output pair can be left floating.
30	VDD	Power	Power supply.
31	VDD	Power	Power supply.
32	nQ3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating.
33	Q3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating.
34	nQ2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating.
35	Q2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating.
36	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.

37	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
38	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
39	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
40	VDD	Power	Power supply.

Table 2: Input Selection Table

IN_SEL	CLOCK INPUT
0	CLK0,nCLK0
1	CLK1,nCLK1

Table 3: Input Select Control Pin

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 Voltage	VDD-0.4		VDD	V
V_{IL}	Logic 0 Voltage	GND		1	V
I_{IH}	Logic 1 Current			100	uA
I_{IL}	Logic 1 Current			0.6	mA
	Capacitance		2		pF

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics

At VDD = 3.3 V and TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

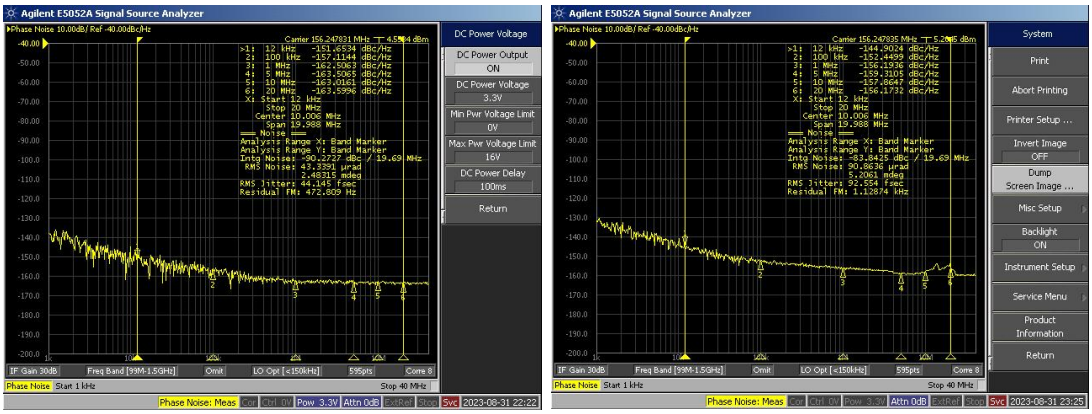
Parameter		Test Conditions	Min	Typ	Max	Unit
DC input characteristics						
V_{ICM}	Input Common-Model Voltage		1.5		VDD-0.1	V
V_{ID}	Input Differential Voltage	±1.7V between input pins	0.4		3.4	V_{P-P}
R_{IN}	Input Resistance	Differential Mode		100		Ω
		Single-Ended Mode		50		
I_{Bias}	Input Bias Current			20		μA
C_{IN}	Input capacitance			0.4		pF
DC output characteristics						
V_{OH}	Output High Voltage	Load=50Ω to(VDD-2.0V)	VDD-1.26		VDD-0.76	V
V_{OL}	Output Low Voltage	Load=50Ω to(VDD-2.0V)	VDD-1.99		VDD-1.54	
V_o	Output Voltage, Single-Ended	V_{OH}-V_{OL}, output static	610		960	mV
V_{REF}	Voltage Reference					
	Output Voltage	-500 μA to +500 μA		(VDD+1)/2		V
	Output Resistance	-500 μA to +500 μA		235		Ω

Electrical Characteristics(Continued)

VCC = 3.3 V; TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
AC PERFORMANCE						
F_{OUT}	Output Frequency		0.1		2000	MHz
I_{DD}	Power Supply Current			550		mA
T_R/T_F	Output Rise/Fall Time	20% to 80%		120	500	ps
T_{PD}	Propagation Delay			500	1500	ps
$T_{SK,O}$	Output skew			20	50	ps
$T_{sk,pp}$	Part-to-Part Skew				500	ps
T_{RJIT}	Additive jitter	Additive RMS phase jitter @ 156.25MHz: (12kHz - 20MHz)		81		fs

PHASE JITTER



(a)Jitter_Source **(b)3V3_156M25_LVPECL**

Figure 1 .RMS_Jitter_3V3=Sqrt(92²-44²)=81fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

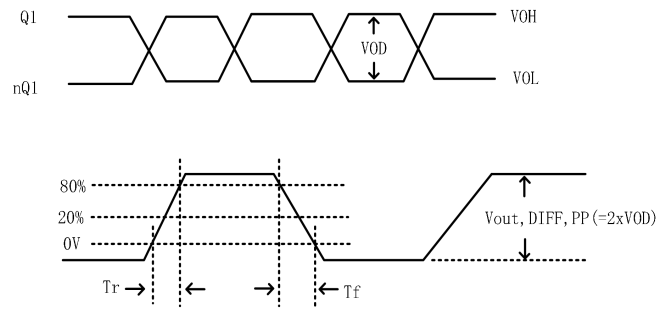
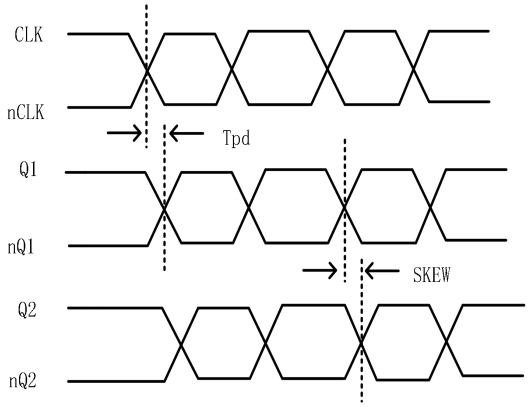


Figure 2.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 3.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

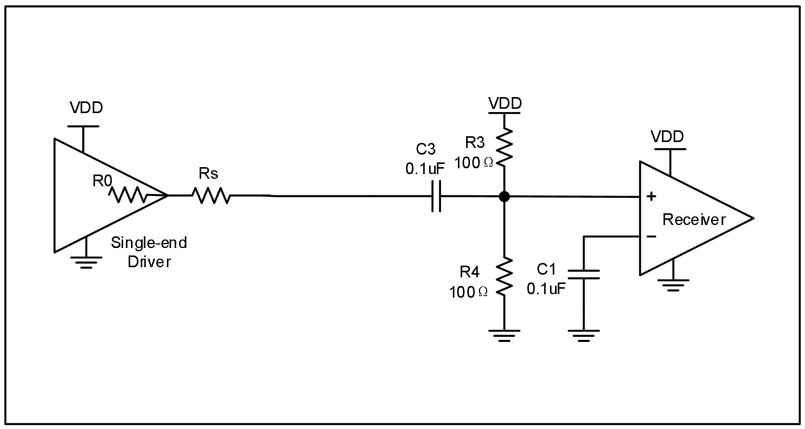
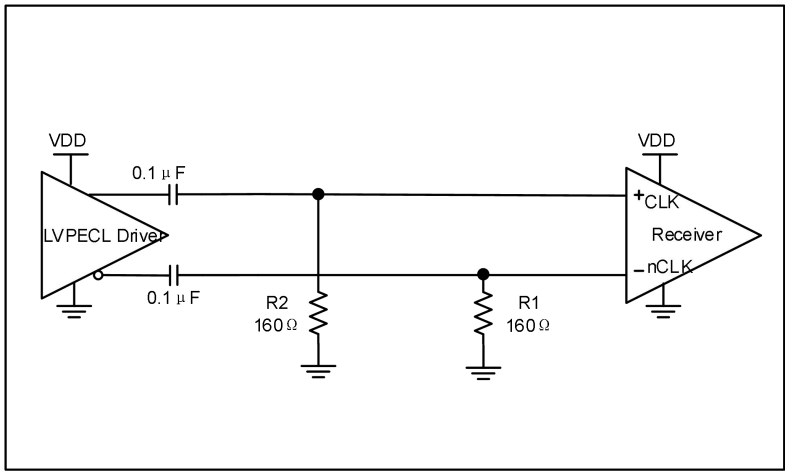
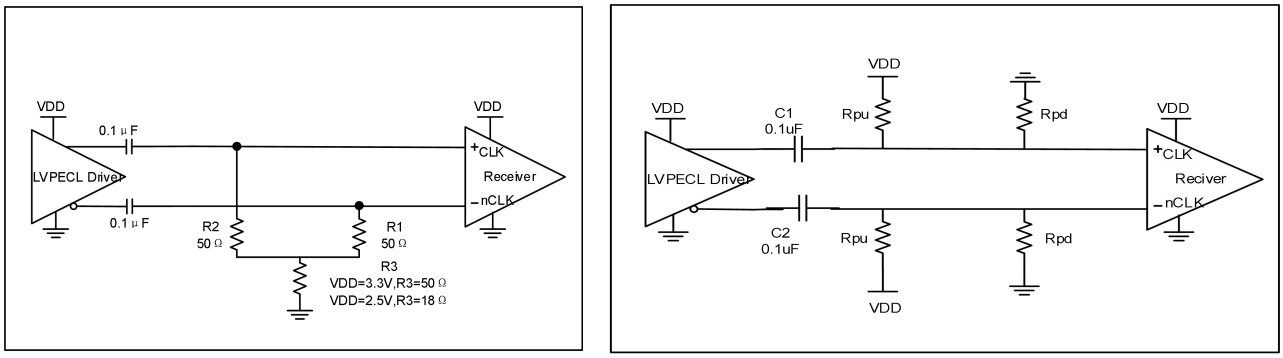


Figure4.Single-termination method of differential input

Input connection circuit

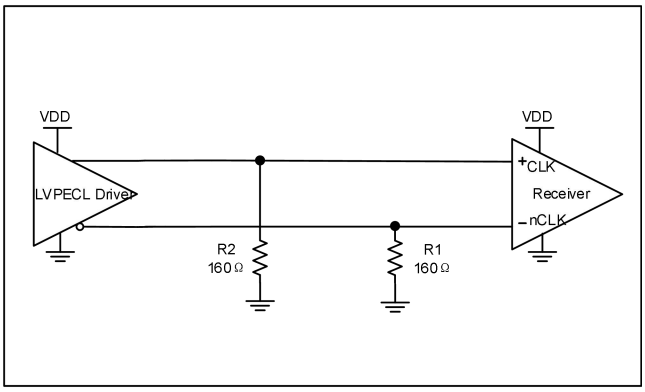
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

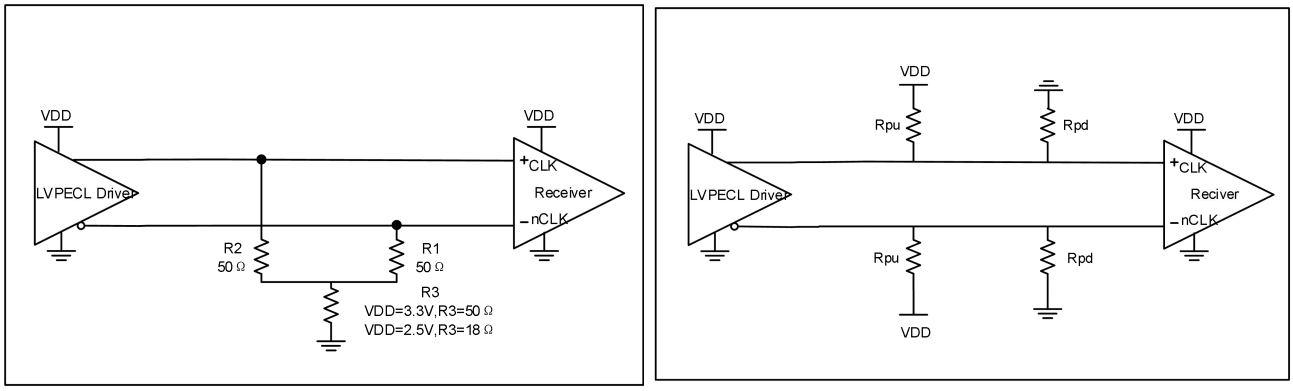




VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

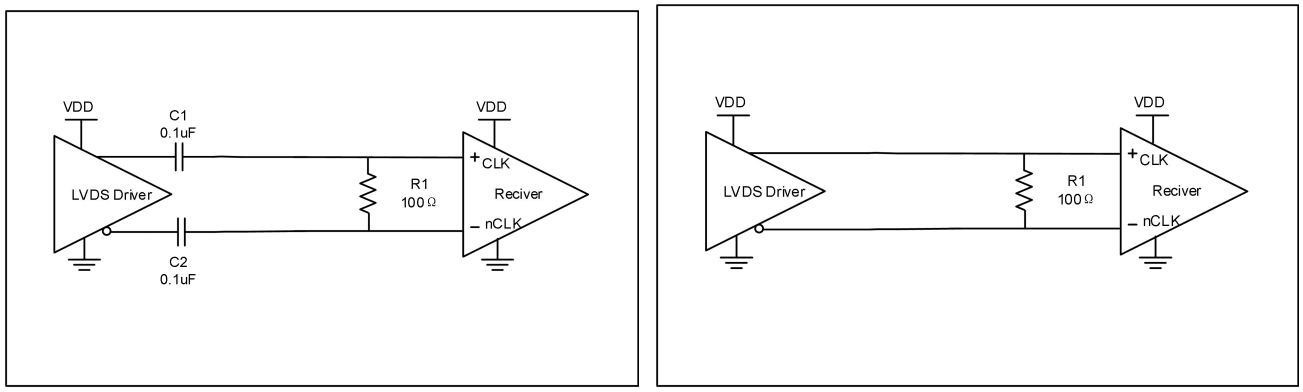
Figure5.LVPECL Driver(AC)





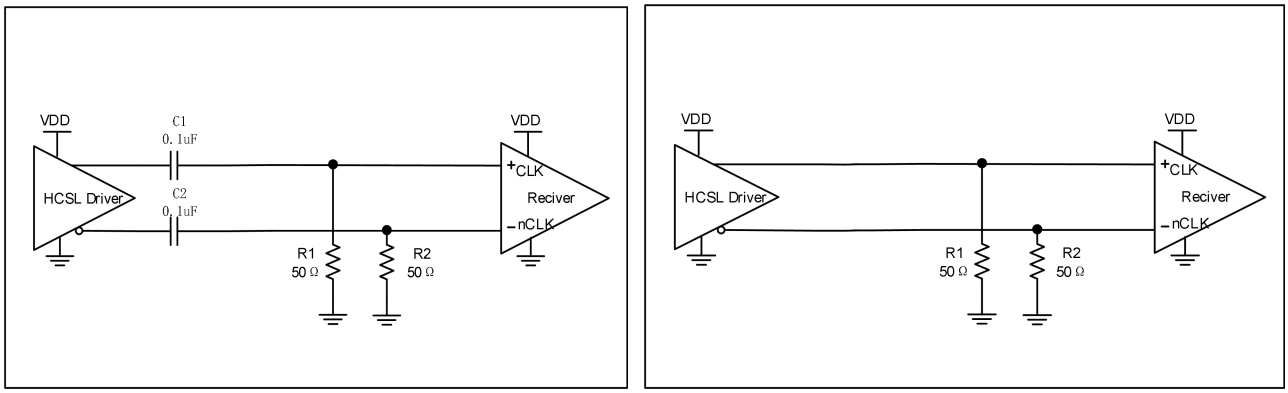
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure6.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

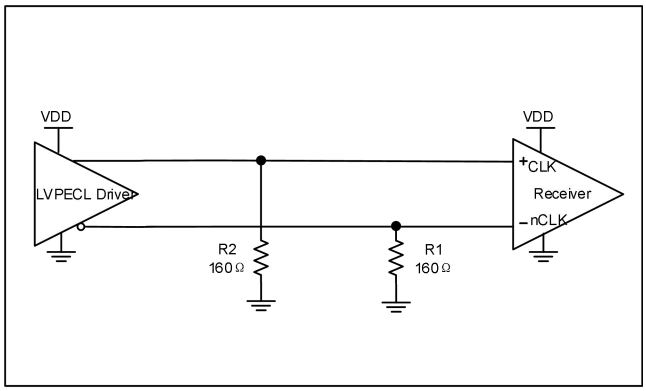
Figure7.LVDS Driver

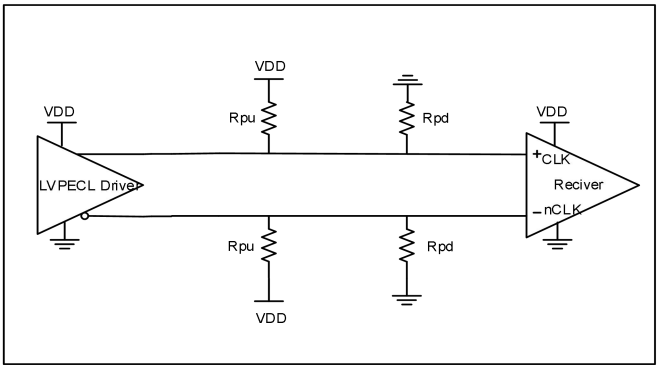


a)AC coupling **b)DC coupling**

Figure8.HCSL Driver

Output connection circuit





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

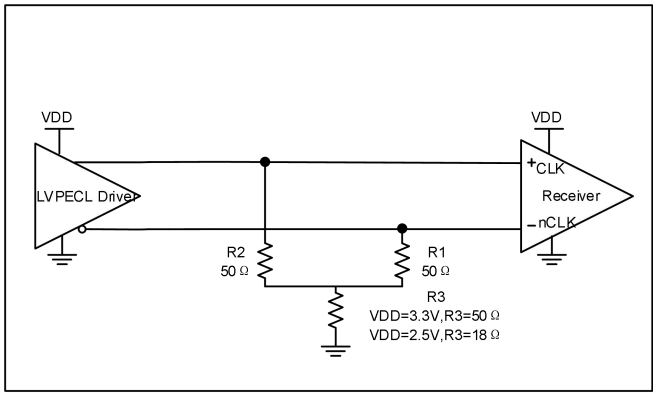
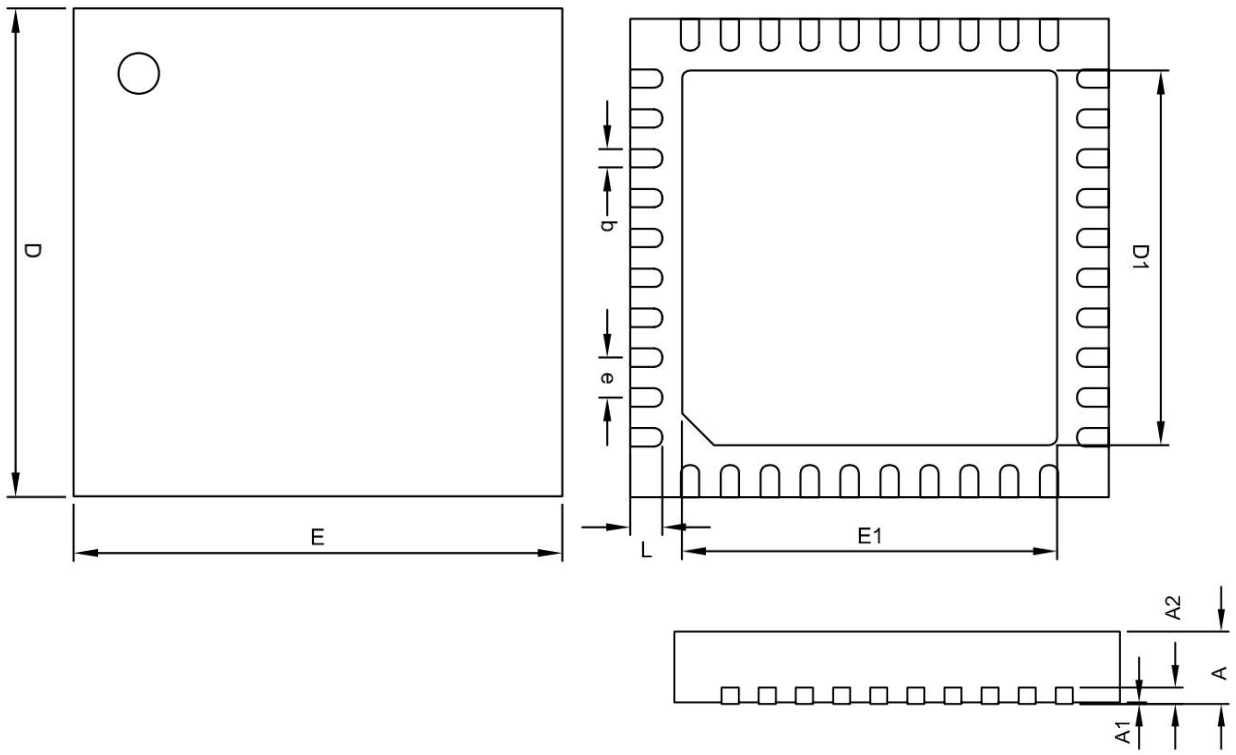


Figure9.LVPECL Driver

PACKAGE DIMENSIONS(QFN-40)



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.55	4.65	4.75	0.1791	0.1831	0.1870
E1	4.55	4.65	4.75	0.1791	0.1831	0.1870
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Note：

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

Reflow profile

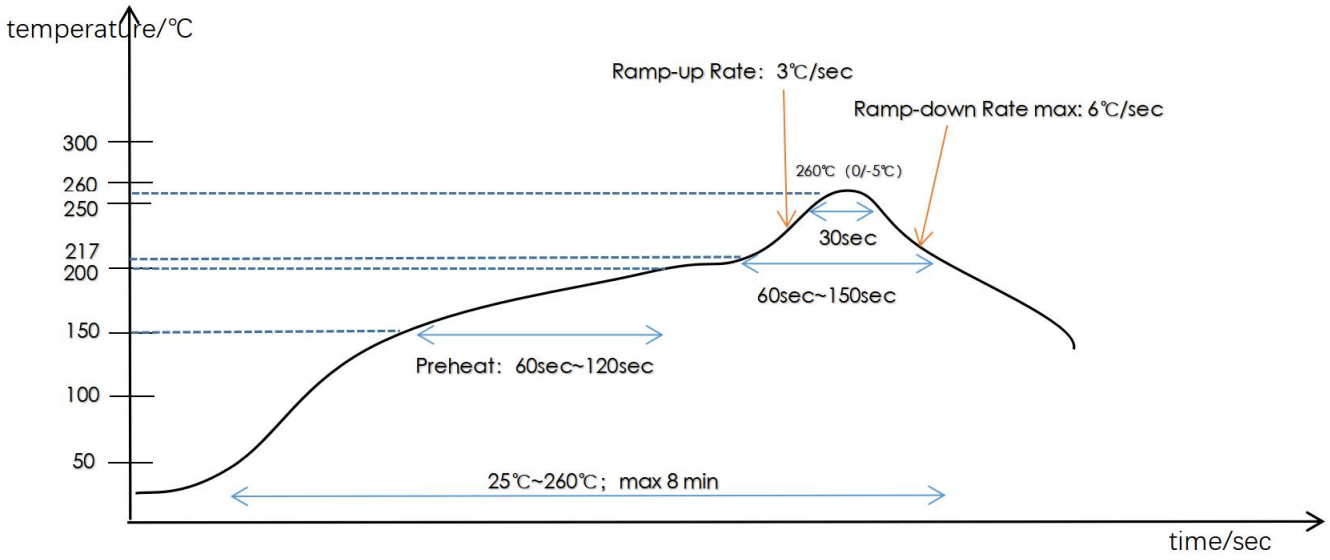


Figure10: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.07.10	First Draft.	1.0
2023.08.29	Modify the PIN pin diagram.	1.5