

## Description

The US5D102 is a 2-GHz, 2-output differential high-performance clock fanout buffer.

The input clock is a differential input. The selected input clock is distributed to a LVPECL differential output.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

## Applications

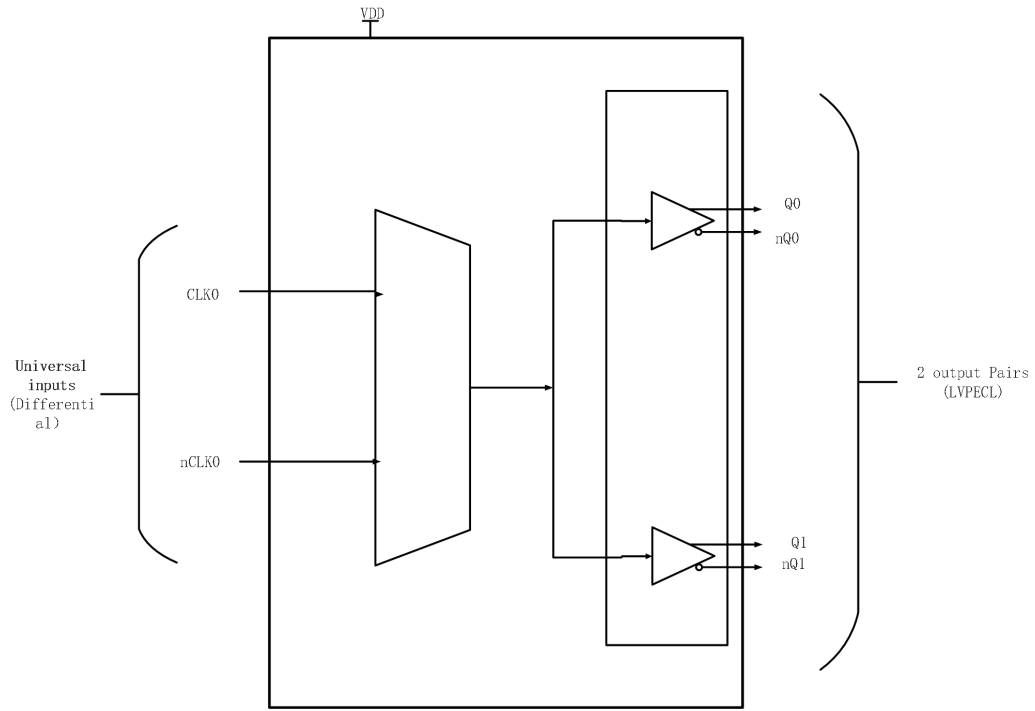
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH, CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express (PCIe 3.0, 4.0, 5.0)
- Remote Radio Units and Baseband Units

## Features

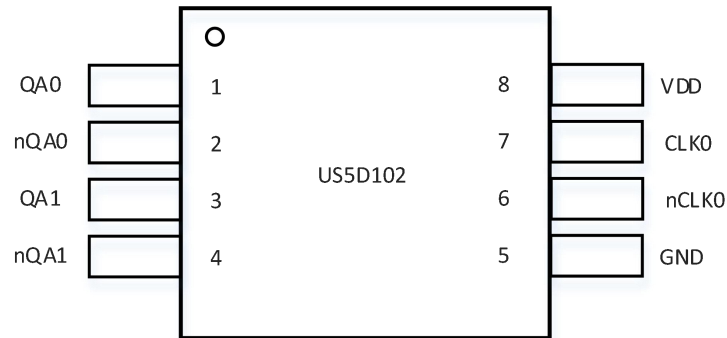
- A differential clock input pairs
- Maximum Output Frequency LVPECL - 2GHz
- Two differential output pairs that can be configured as LVPECL
- Output skew: 20ps (typical)
- Part-to-part skew: 300ps (Maximum)
- Additive RMS phase jitter @ 156.25MHz: 80fs RMS (10kHz - 20MHz), typical @ 3.3V/3.3V
- Supply voltage mode: VDD=3.3V or 2.5V
- Industrial Temperature Range: -40°C to 85°C
- Available in 8-pin TSSOP package



## Block Diagram



**Pin Assignment for 8-pin TSSOP Package**



## Pin Description and Pin Characteristic Tables

**Table 1: Pin Descriptions<sup>1</sup>**

Number	Name	Type	Description
1	QA0	Output	Differential clock output pair. LVPECL
2	nQA0	Output	Differential clock output pair. LVPECL
3	QA1	Output	Differential clock output pair. LVPECL
4	nQA1	Output	Differential clock output pair. LVPECL.
5	GND	Power	Ground.
6	nCLK0	Input	Inverting differential clock. Internally biased to $0.5V_{DD}$ .
7	CLK0	Input	Non-inverting differential clock. Internally biased to ground.
8	$V_{DD}$	Power	Power supply for Core and input Buffer blocks, 3.3V or 2.5V.

## Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
$V_{DD}$	4.6V
$V_{IN}$	-0.3V to $V_{DD} + 0.3V$
$T_J$ :Junction Temperature	150°C
$T_{STG}$ :Storage Temperature	-65°C to 150°C

## ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

## Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>A</sub>	Ambient air temperature	-40		85	°C
T <sub>J</sub>	Junction temperature			125	°C
V <sub>DD</sub>	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

## Electrical Characteristics

Unless otherwise specified: V<sub>DD</sub> = 3.3 V ± 5%, -40 °C ≤ T<sub>A</sub> ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Current Consumption<sup>(2)</sup></b>					
I <sub>DD_CORE</sub>	Core Supply Current, All Outputs Disabled	CLK_0 selected	11.5		mA
I <sub>DD_PECL</sub>	Additive Core Supply Current, LVPECL Output Disabled		31.7		mA
I <sub>DDO_PECL</sub>	Additive Output Supply Current, LVPECL Output Disabled	Includes Output Bias and Load Currents, R <sub>T</sub> = 50 Ω to V <sub>DD</sub> - 2V	188		mA

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) See [Power Considerations](#) for more information on current consumption and power dissipation calculations.
- (3) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the V<sub>DDO</sub> supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) =  $\left[ \frac{2 * 10^{(PSRR / 20)}}{\pi * f_{CLK}} \right] * 1E12$

## Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>Universal Clock Inputs (CLK0/nCLK0, CLK1/nCLK1)</b>						
f <sub>CLKin</sub>	Input Frequency Range <sup>(4)</sup>	Functional up to 2-GHz	0.1		2000	MHz
V <sub>IHD</sub>	Differential Input High Voltage	CLKin driven differentially			VDD	V
V <sub>ILD</sub>	Differential Input Low Voltage				GND	V
V <sub>ID</sub>	Differential Input Voltage Swing <sup>(5)</sup>		0.15		1.3	V
V <sub>CMD</sub>	Differential Input Common Mode Voltage	V <sub>ID</sub> = 150 mV	0.25		VDD - 1.2	V
		V <sub>ID</sub> = 350 mV	0.25		VDD - 1.1	
		V <sub>ID</sub> = 800 mV	0.25		VDD - 0.9	
V <sub>IH</sub>	Single-Ended Input High Voltage	CLK_X driven single-ended (AC or DC coupled), nCLK_X AC coupled to GND or externally biased within V <sub>CM</sub> range			VDD	V
V <sub>IL</sub>	Single-Ended Input Low Voltage				GND	V
V <sub>I_SE</sub>	Single-Ended Input Voltage Swing <sup>(6)(7)</sup>		0.3		2	V <sub>pp</sub>
V <sub>CM</sub>	Single-Ended Input Common Mode Voltage		0.25		VDD - 1.2	V
IEE	Working current	F <sub>IN</sub> =20MHz, VDD=3.3V			220	mA
		F <sub>IN</sub> =20MHz, VDD=2.5V			190	

(4) Specification is ensured by characterization and is not tested in production.

(5) See V<sub>ID</sub> = Differential input Voltage Swing, V<sub>OD</sub> = Differential output Voltage Swing.

(6) Parameter is specified by design, not tested in production.

(7) For clock input frequency ≥ 100 MHz, CLK\_X can be driven with single-ended (LVCMOS) input swing up to 3.3 V<sub>pp</sub>. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 V<sub>pp</sub> max to prevent input saturation.

## Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>LVPECL Outputs</b>						
f <sub>CLKout</sub>	Maximum Output Frequency	VDD=3.3V, R <sub>T</sub> = 160 Ω to GND	0.1		2000	MHz
Jitter <sub>ADD</sub>	Additive RMS Jitter	CLKin: 156.25 MHz (10kHz-20MHz)		80	120	fs
DUTY	Duty Cycle <sup>(4)</sup>	50% input clock duty cycle	45%		55%	
V <sub>OH</sub>	Output High Voltage	T <sub>A</sub> = 25 °C, DC Measurement, R <sub>T</sub> = 50 Ω to VDDO - 2 V	VDDO - 1.2	VDDO - 0.99	VDDO - 0.7	V
V <sub>OL</sub>	Output Low Voltage		VDDO - 2.0	VDDO - 1.75	VDDO - 1.5	V
V <sub>OD</sub>	Output Voltage Swing <sup>(5)</sup>		600	760	1000	mV
t <sub>R</sub>	Output Rise Time 20% to 80% <sup>(6)</sup>	R <sub>T</sub> = 160 Ω to GND, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R <sub>L</sub> = 100 Ω differential, C <sub>L</sub> ≤ 5 pF		200	500	ps
t <sub>F</sub>	Output Fall Time 80% to 20% <sup>(6)</sup>			200	500	ps

- (8) See *Typical Characteristics* for output operation over frequency.  
 (9) For the 156.25 MHz clock input conditions, Additive RMS Jitter (J<sub>ADD</sub>) is calculated using Method : J<sub>ADD</sub> = SQRT(J<sub>OUT</sub><sup>2</sup> - J<sub>SOURCE</sub><sup>2</sup>), where J<sub>OUT</sub> is the total RMS jitter measured at the output driver and J<sub>SOURCE</sub> is the RMS jitter of the clock source applied to CLKin.  
 (10) 156.25 MHz LVDS input clock source from Epson SG3225VEN(LVDS) Low-Noise SPXO.  
 (11) 156.25 MHz LVPECL input clock source from Epson SG3225VEN(LVPECL) Low-Noise SPXO.  
 (12) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz.  
 (13) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

## Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, CLKin driven differentially, input slew rate ≥ 3 V/ns, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>Propagation Delay and Output Skew</b>						
t <sub>PD_PECL</sub>	Propagation Delay CLKin-to-LVPECL <sup>(6)</sup>	R <sub>T</sub> = 160 Ω to GND, R <sub>L</sub> = 100 Ω differential, C <sub>L</sub> ≤ 5 pF		0.5	1.5	ns
t <sub>SK(O)</sub>	Output Skew LVPECL <sup>(4) (15) (17)</sup>	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.		20	50	ps
t <sub>SK(PP)</sub>	Part-to-Part Output Skew LVPECL <sup>(6) (15) (17)</sup>				300	ps

- (14) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

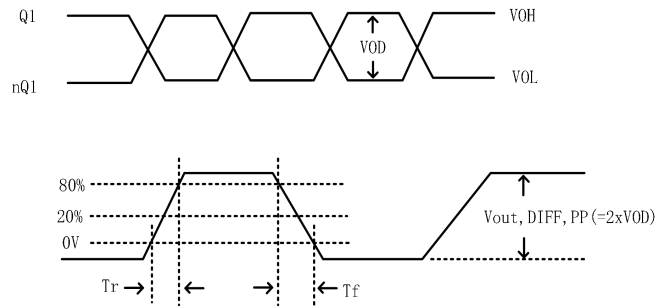
# PHASE JITTER



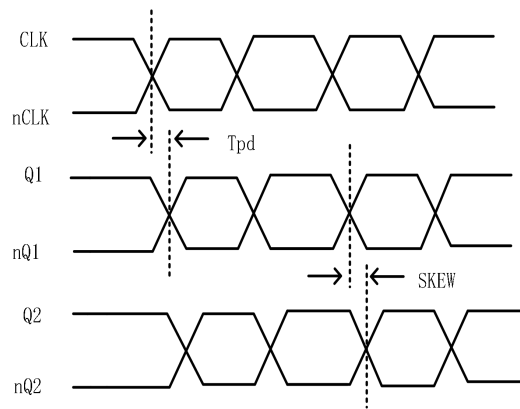
Figure 1 .RMS\_Jitter\_3V3=√(93<sup>2</sup>-48<sup>2</sup>)=80fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

## Timing Diagrams



**Figure 2.output voltage and rise/fall time**



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, \dots, 7$ ), or as the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 7$ ).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, \dots, 7$ ) across multiple devices, or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 7$ ) across multiple devices

**Figure 3.output and skew**

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal,  $R_s$  and  $R_0$  in the driver form a  $50\ \Omega$  impedance match, and the direct-isolated capacitor  $C_3$  avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to  $V_{DD}/2$ .

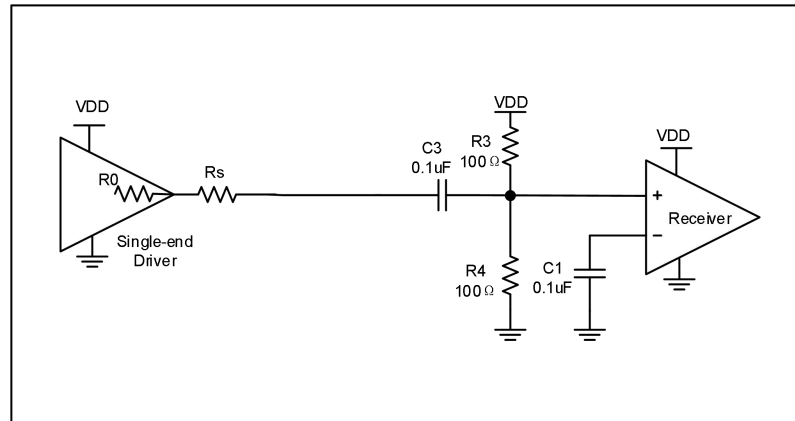
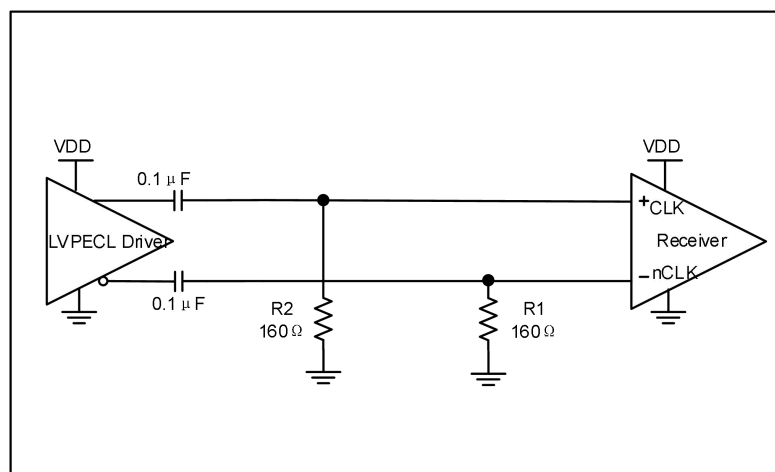
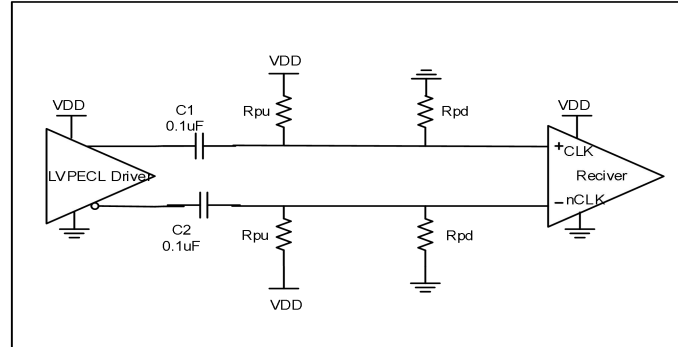
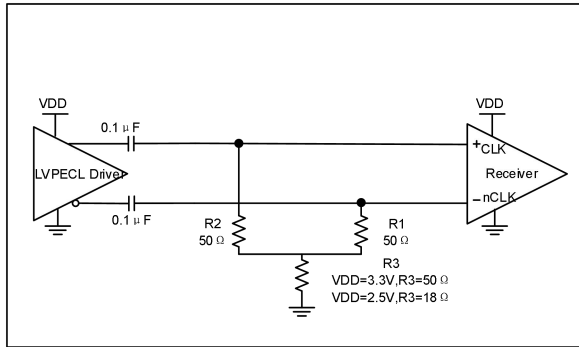


Figure4.Single-termination method of differential input

### Input connection circuit

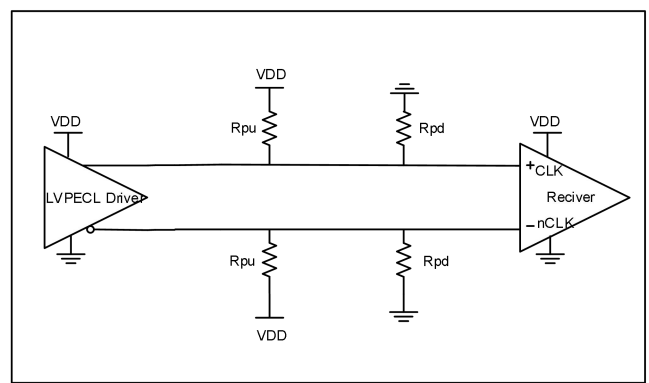
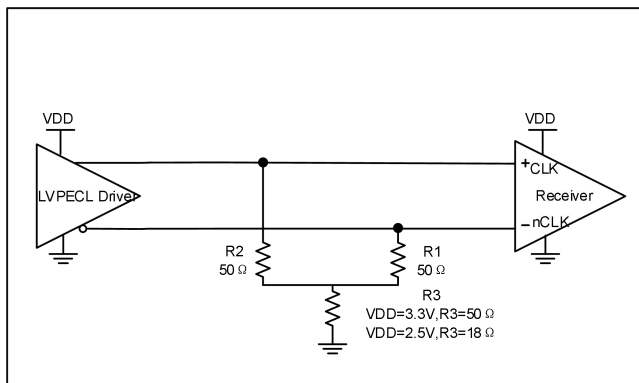
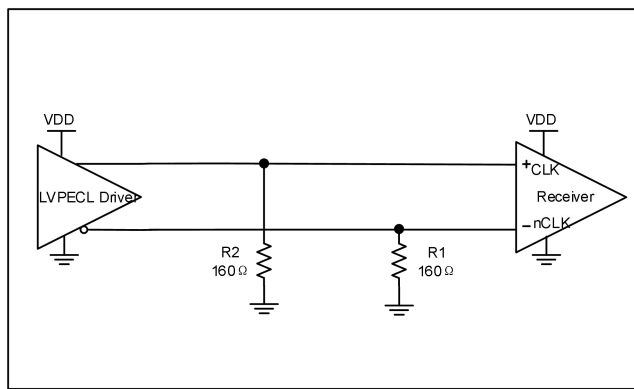
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figure5 to Figure8 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.





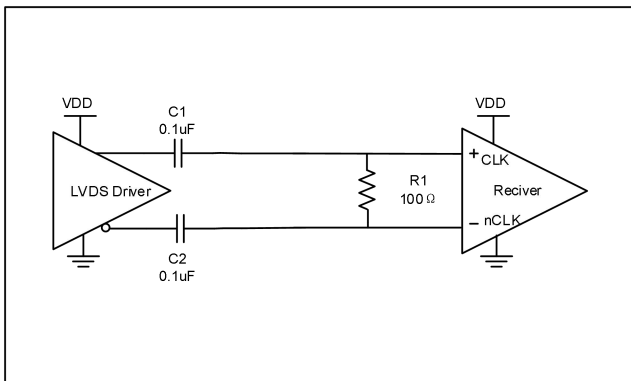
VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(AC)

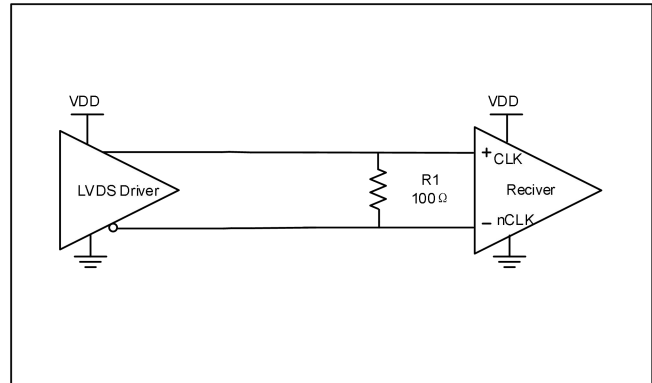


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure6.LVPECL Driver(DC)

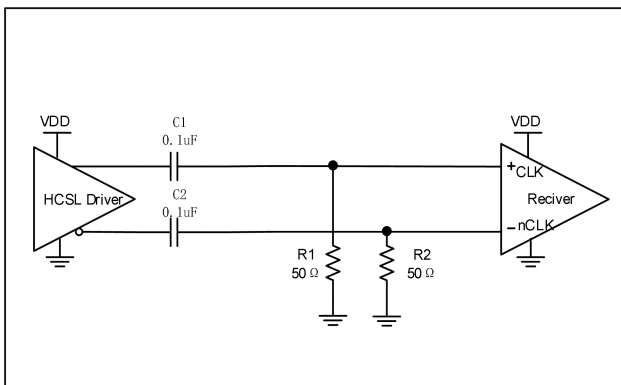


a)AC coupling

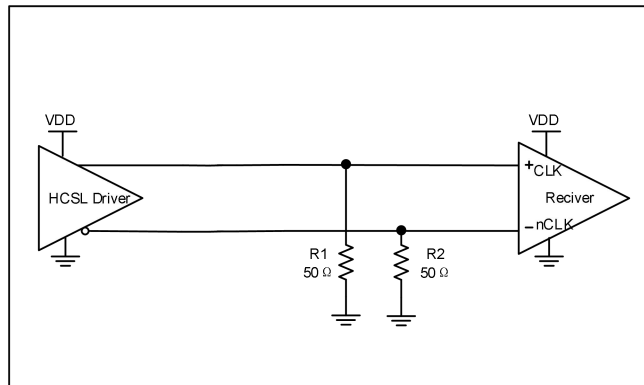


b)DC coupling

Figure7.LVDS Driver



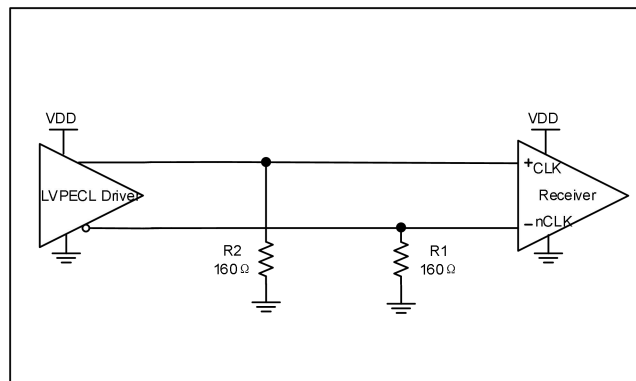
a)AC coupling

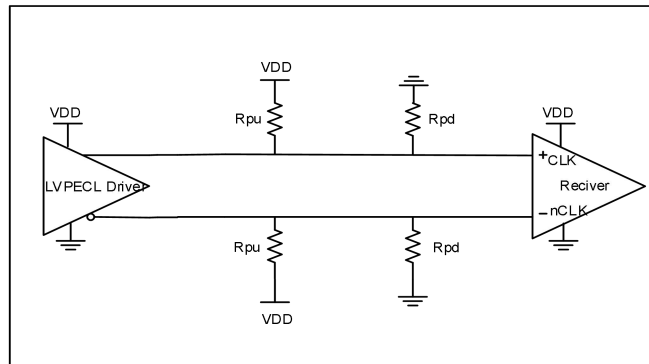


b)DC coupling

Figure8.HCSSL Driver

### Output connection circuit





VDD	Rpu	Rpd
3.3V	120 $\Omega$	82 $\Omega$
2.5V	250 $\Omega$	62.5 $\Omega$

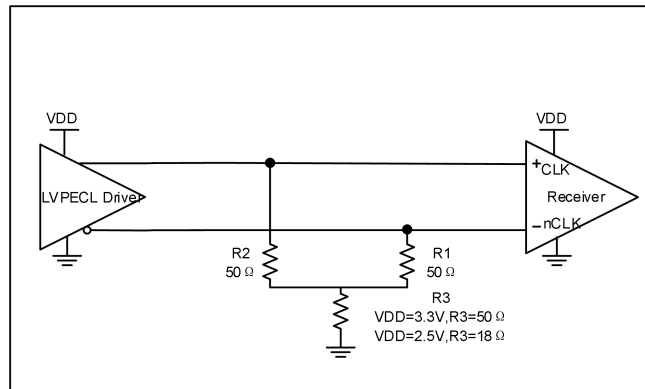
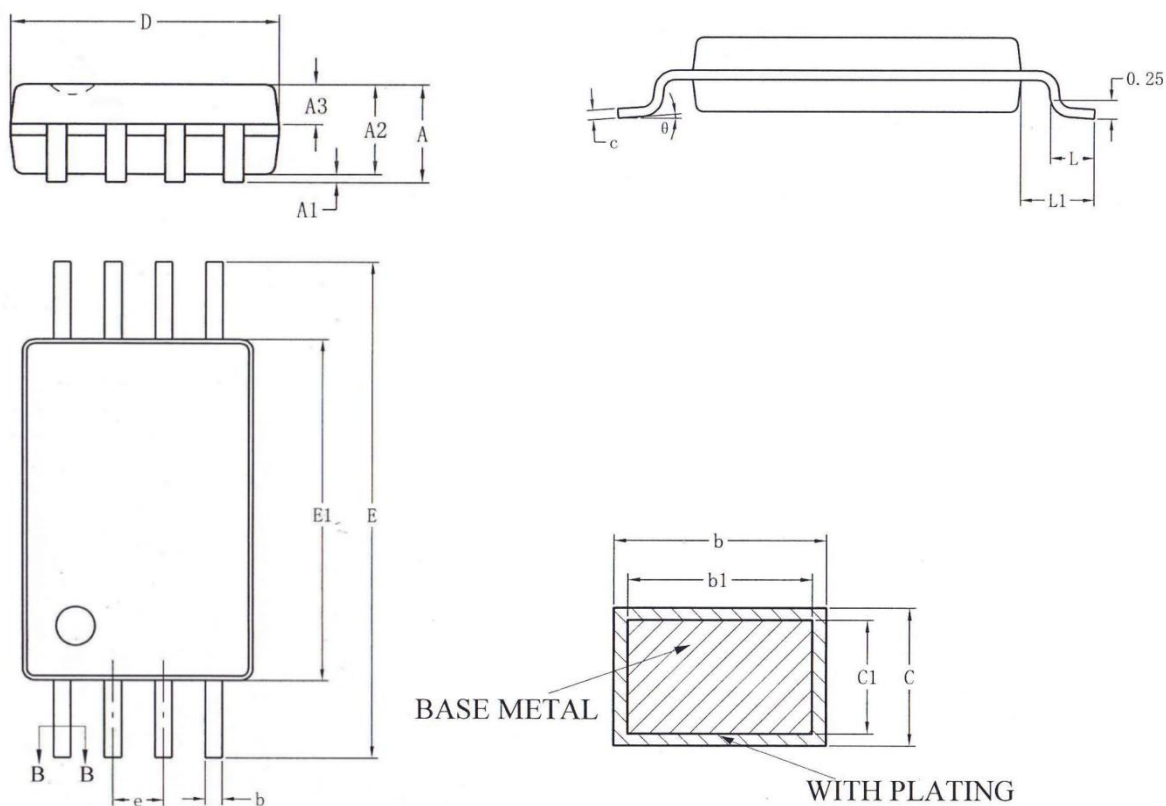


Figure9.LVPECL Driver

## PACKAGE DIMENSIONS



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	-	0.75
L1	1.00REF		
$\theta$	0	-	8°

## Reflow profile

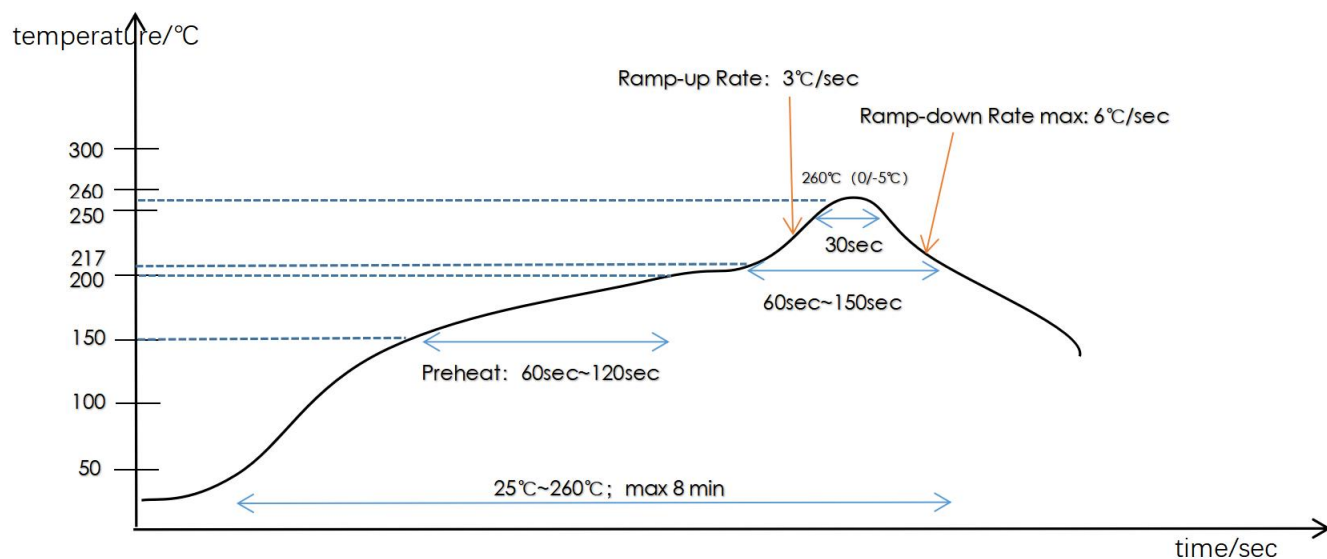
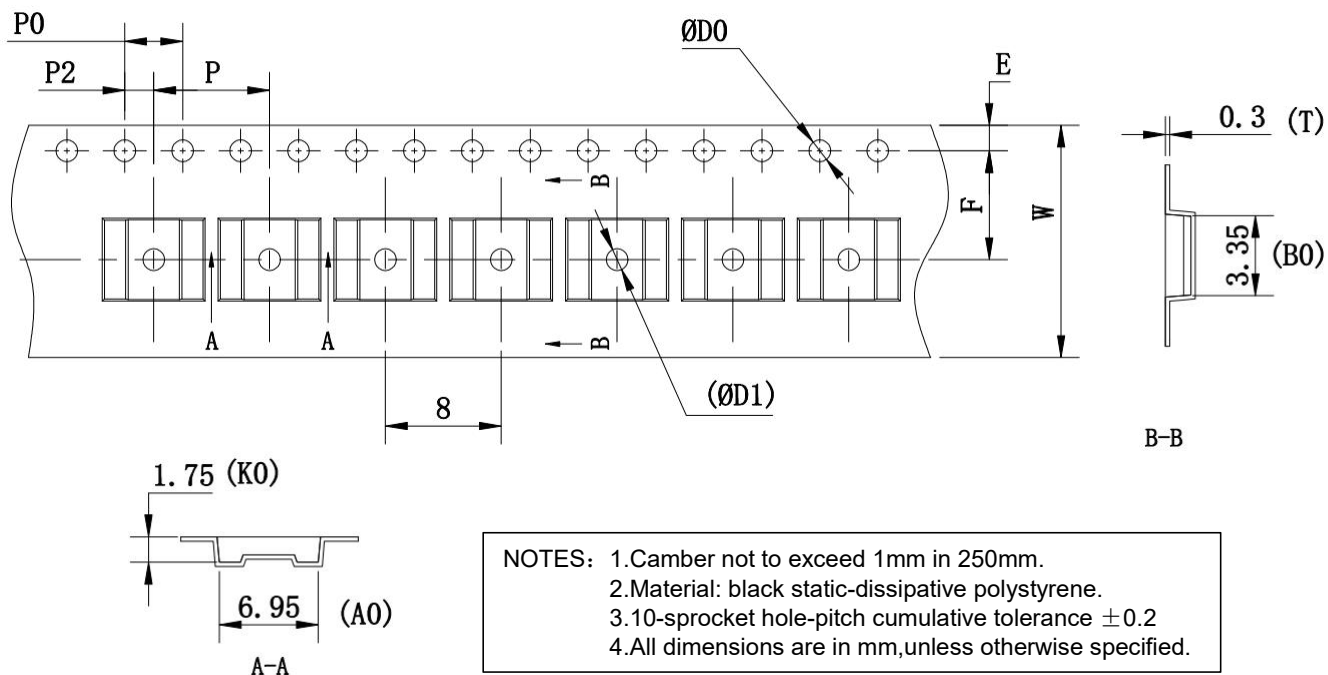


Figure10: Recommended Temperature(PB-Free)

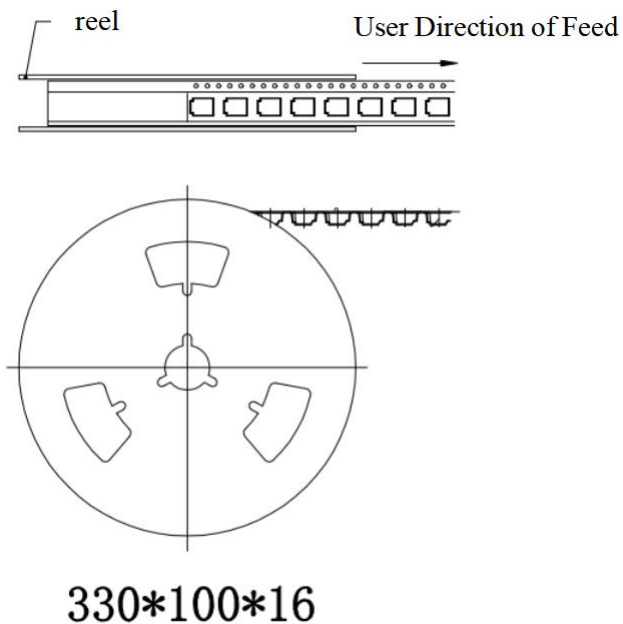
Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

## Tape and Reel information

### Tape:



### Reel:



## Revision History

Date	Description of Change	Revision
2022.08.18	First Draft.	1.0
2022.09.02	Add PCI-E5.0	2.0