Description

The US5D204 is a low skew, high performance 2-to-4 clock fanout buffer. Utilizing Low Voltage Differential Signaling (LVDS) the US5D204 provides a low power, low noise, solution for distributing clock signals. The US5D204 accepts any differential input level and translates it to 3.3V, 2.5V LVDS output levels. Guaranteed output and part-to-part skew characteristics make the US5D204 ideal for those applications demanding well defined performance and repeatability.

The US5D204 clock buffer distributes one of two selectable clock inputs to 4 pairs of differential LVDS clock outputs with minimum skew for clock distribution. The US5D204 can accept two clock sources into an input multiplexer. The inputs can either be LVDS,LVPECL, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal.

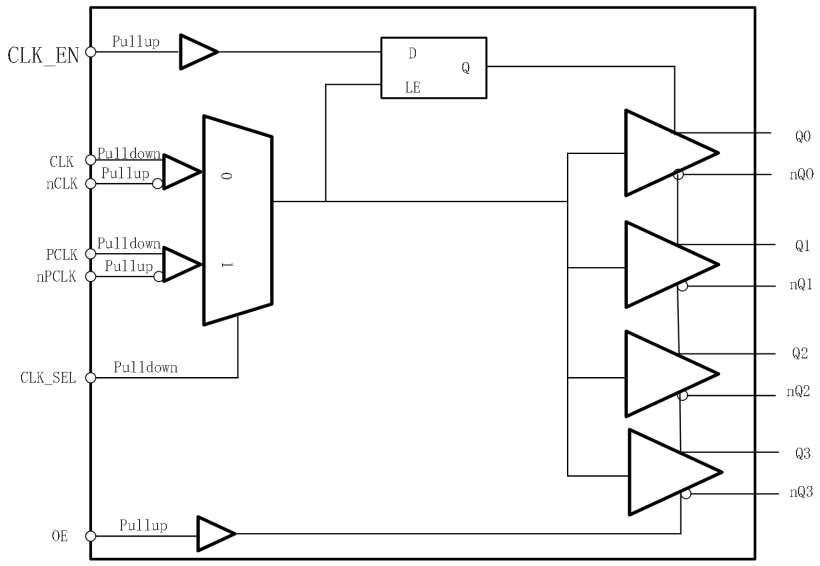
Features

- 2:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS and LVCMOS
- Four LVDS outputs
- Maximum Output Frequence LVDS - 2-GHz
- Propagation Delay: 0.4 ns(typical)
- Output skew: 50 ps (Maximum)
- Part-to-part skew: 300 ps(Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz: 50 fs RMS (10kHz - 20MHz)
- 3.3V, 2.5V operating supply
- Industrial Temperature Range:-40°C to 85°C
- Available in TSSOP-20 package

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram



Pin Assignment for TSSOP-20 Package

Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
9	GND	Power	Ground.
13	GND	Power	Ground.
2	CLK_EN	Input	Synchronous clock enable. When HIGH clock outputs follows clock input. When LOW, Q outputs are force low, nQ outputs are force high.
3	CLK_SEL	Input	Clock select input. When HIGH selects differential PECL inputs.When LOW selects differential HSTL inputs.
4	CLK	Input	Non-inverting differential clock input.
5	nCLK	Input	Inverting differential clock input.
6	PCLK	Input	Non-inverting differential clock input.
7	nPCLK	Input	Inverting differential clock input.
8	OE	Input	Output enable. Controls enabling and disabling of outputs Q0, nQ0 thru Q3, nQ3.
10	VDD	Power	Power supply pin.
18	VDD	Power	Power supply pin.
11	Q3	Output	Differential output pair number 3.
12	nQ3	Output	Differential output pair number 3.
14	Q2	Output	Differential output pair number 2.
15	nQ2	Output	Differential output pair number 2.
16	Q1	Output	Differential output pair number 1.
17	nQ1	Output	Differential output pair number 1.
19	Q0	Output	Differential output pair number 0.
20	nQ0	Output	Differential output pair number 0.

Table 2A: CONTROL INPUTS FUNCTION TABLE

INPUTS			OUTPUTS	
OE	CLK_EN	CLK_SEL	Q1,Q2,Q3	nQ1,nQ2,nQ3
0	X	X	Hi Z	Hi Z
1	0	0	Low	High
1	0	1	Low	High
1	1	0	ACTIVE	ACTIVE
1	1	1	ACTIVE	ACTIVE

Table 2B: CLOCK INPUTS FUNCTION TABLE

INPUTS		OUTPUTS		Input to Output Mode	Polarity
CLK,PCLK	nCLK,nPCLK	Q0,Q1,Q2,Q3	nQ0,nQ1,nQ2,nQ3		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	See note1	Low	High	Single ended to Differential	Non Inverting
1	See note1	High	Low	Single ended to Differential	Non Inverting
See note1	0	High	Low	Single ended to Differential	Inverting
See note1	1	Low	High	Single ended to Differential	Inverting

NOTE1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1μF capacitor from the input to ground. The resulting switch point is approximately VCC/2 ± 300mV.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C
IEE:Operating current	190mA

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

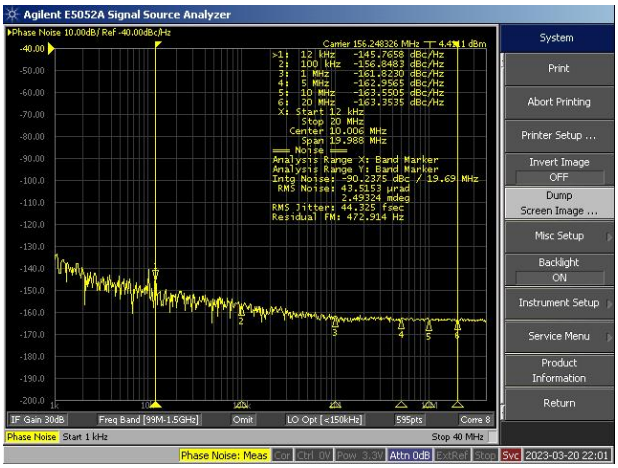
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V

Electrical Characteristics

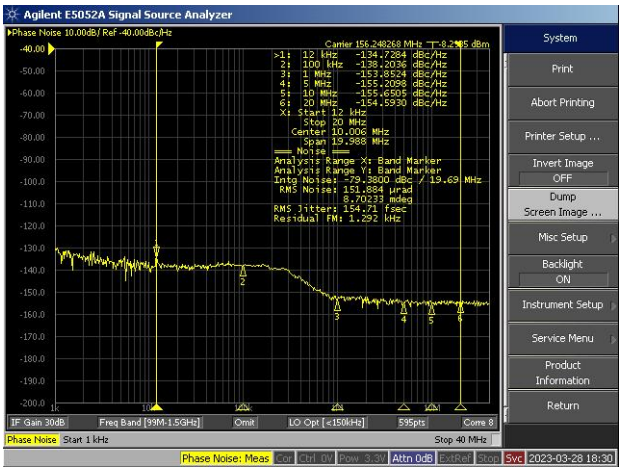
VDD = 3.135 V to 3.465 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
VIH	Input high voltage	CLK_EN,CLK_SEL,OE	2			V
VIL	Input low voltage	CLK_EN,CLK_SEL,OE			0.8	V
IIH	Input high current	CLK_EN,OE			5	μA
		CLK_SEL			150	μA
IIL	Input low current	CLK_EN,OE	-150			μA
		CLK_SEL	-5			μA
LVDS DC CHARACTERISTICS						
VOD	Differential Output Voltage		250	350	450	mV
ΔVOD	VOD Magnitude Change			4	35	mV
VOS	Offset Voltage		1.125	1.25	1.375	V
ΔVOS	VOS Magnitude Change			5	25	mV
AC CHARACTERISTICS						
FIN	Input frequency		0.1		650	MHz
t_{pLH}	Propagation Delay, Low-to-high	0≤f≤650MHz	1.8		2.4	ns
$T_{sk(0)}$	Output skew				50	ps
$T_{sk(pp)}$	Part-to-part skew				300	ps
t_R	Output rise time	RL=100Ω	200	400	600	ps
t_F	Output fall time	RL=100Ω	200	400	600	ps
t_{RJIT}	Phase jitter	@156.25MHz（10KHz-20MHz）,VDD=3.3V		50		fs

PHASE JITTER



(a)Jitter_Source



(b)3V3_156M25_LVDS

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

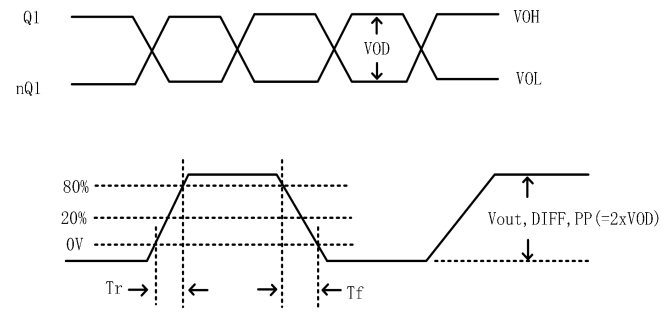
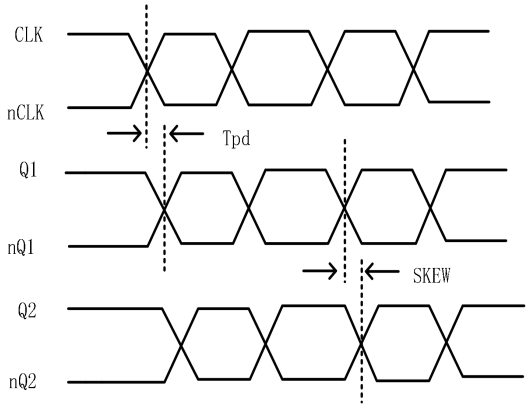


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 2.output and skew

Applications Information

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

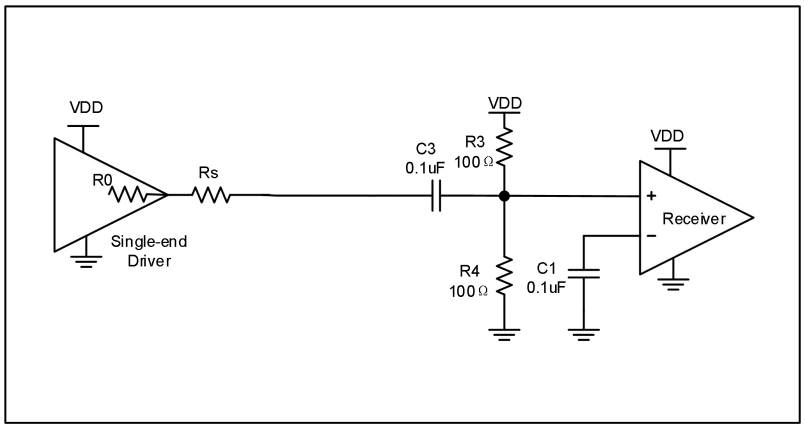
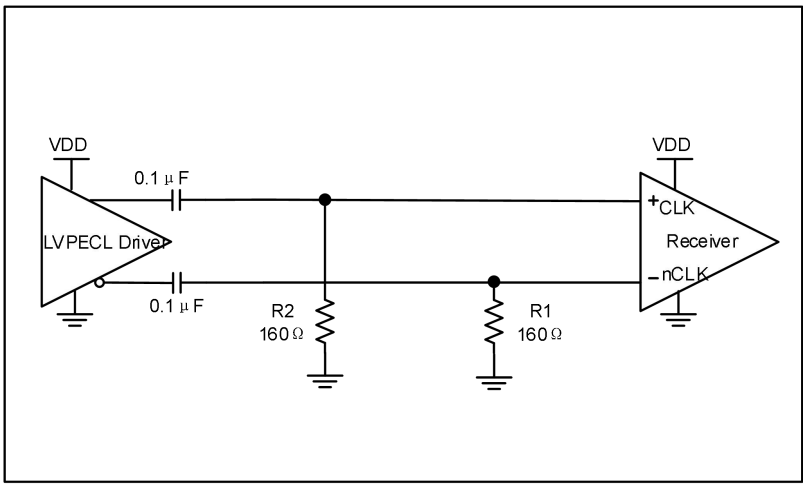
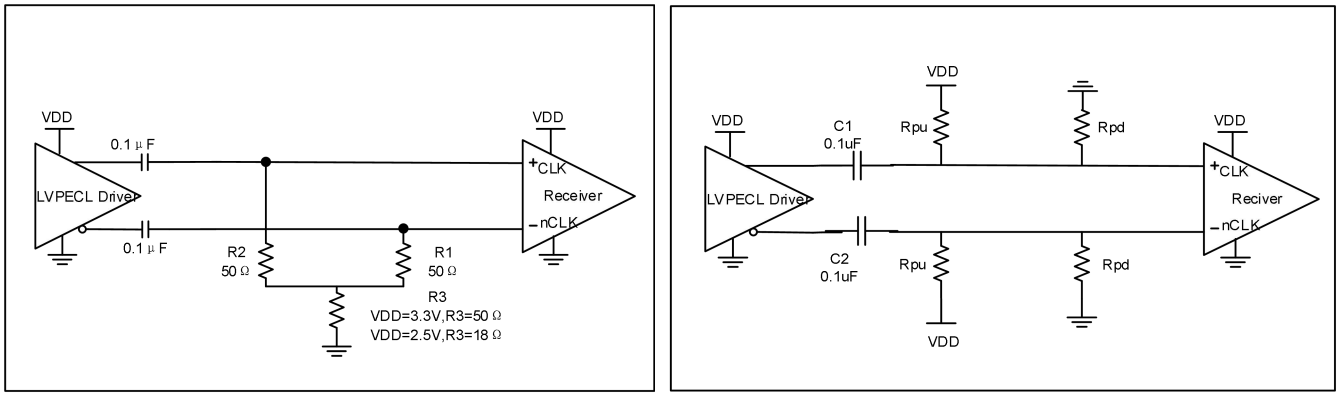


Figure3.Single-termination method of differential input

Input connection circuit

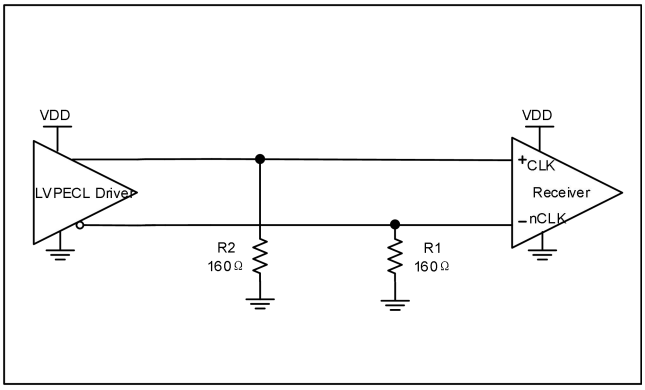
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure4 to Figure7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

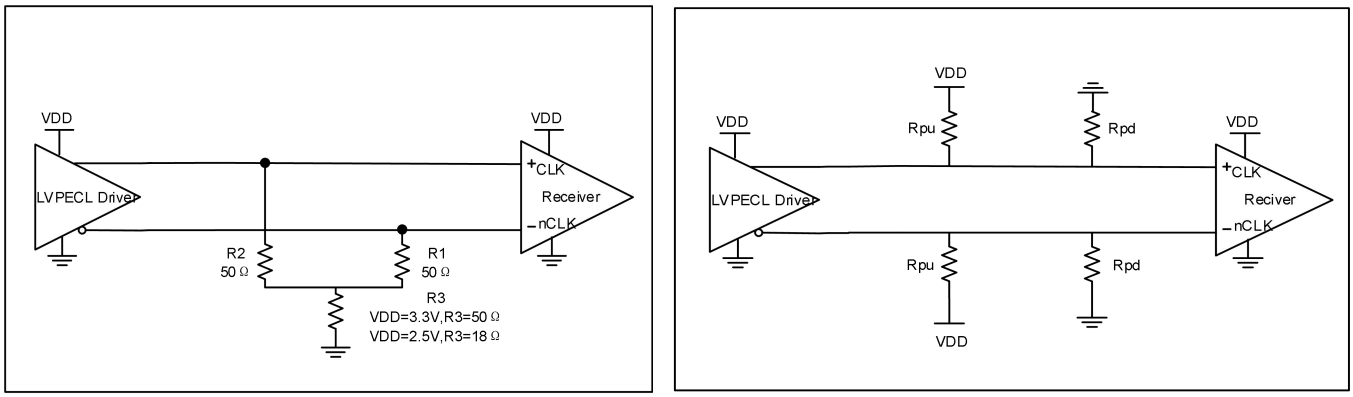




VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

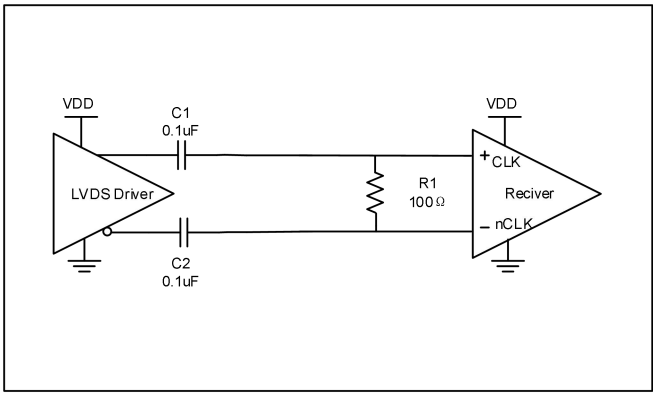
Figure4.LVPECL Driver(AC)

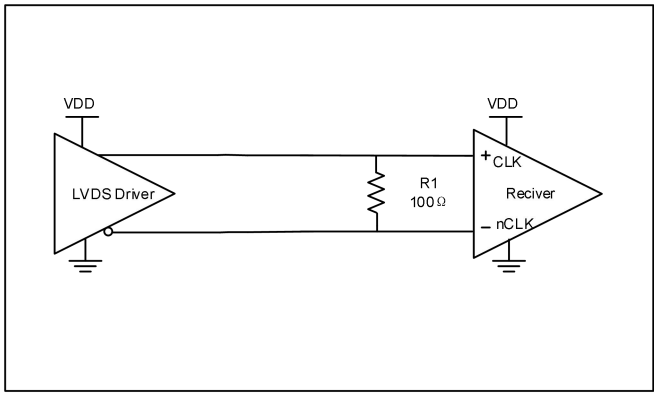




VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

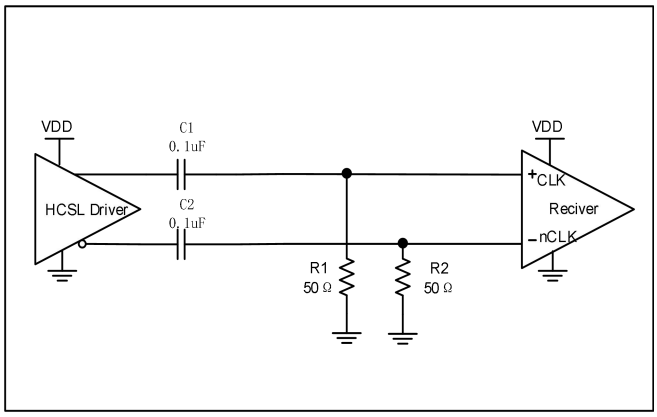
Figure5.LVPECL Driver(DC)

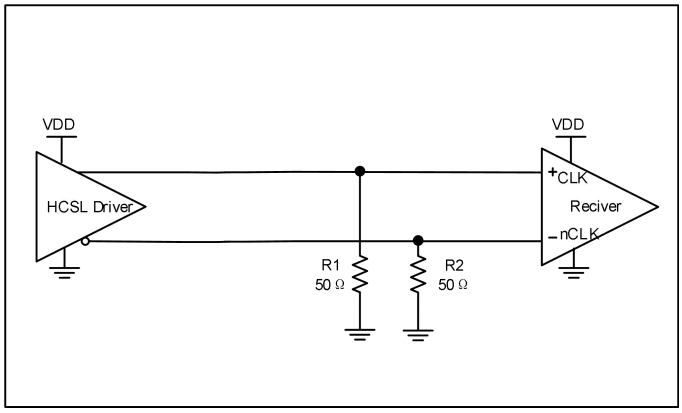




a)AC coupling **b)DC coupling**

Figure6.LVDS Driver

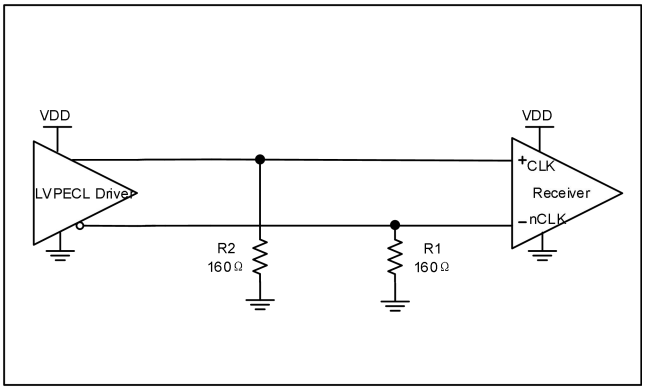


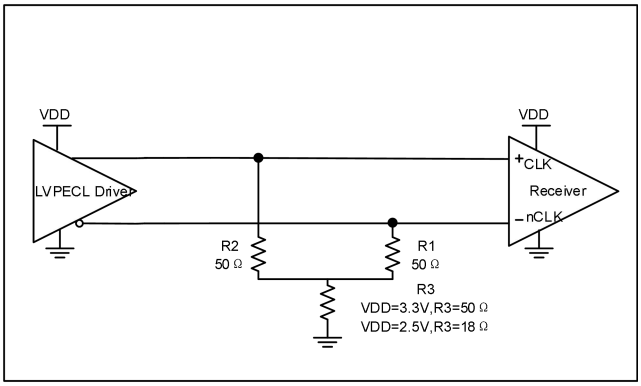


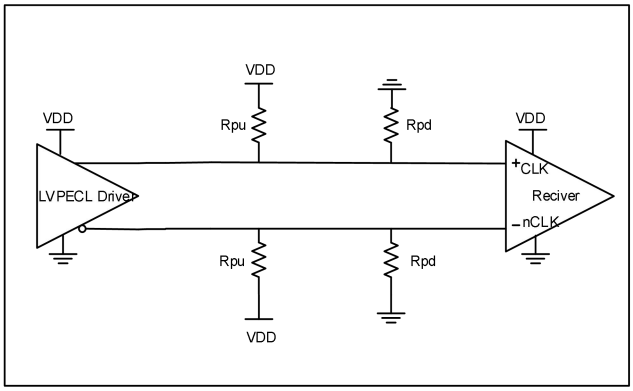
a)AC coupling **b)DC coupling**

Figure7.HCSL Driver

Output connection circuit







VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure8.LVPECL Driver

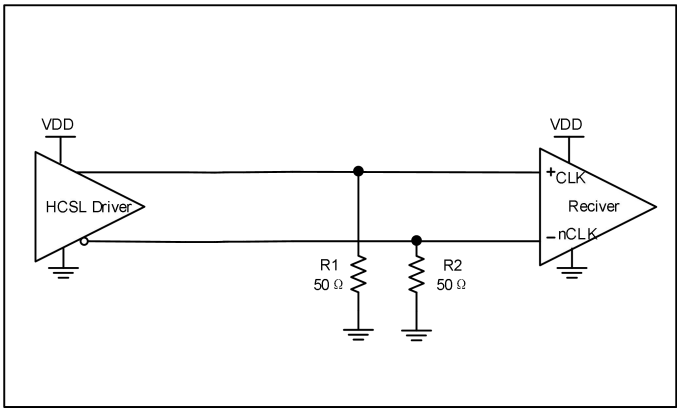


Figure9.HCSL Driver

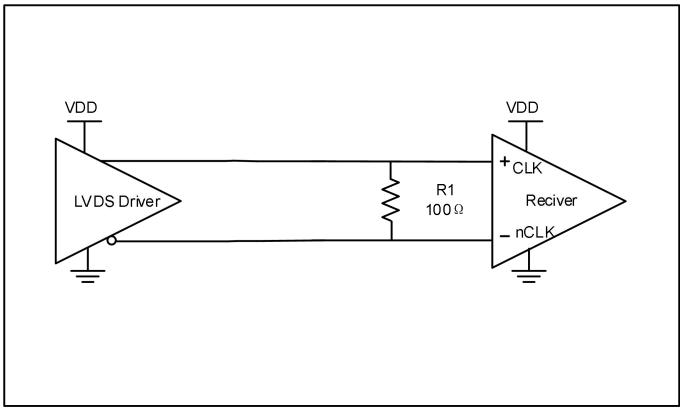
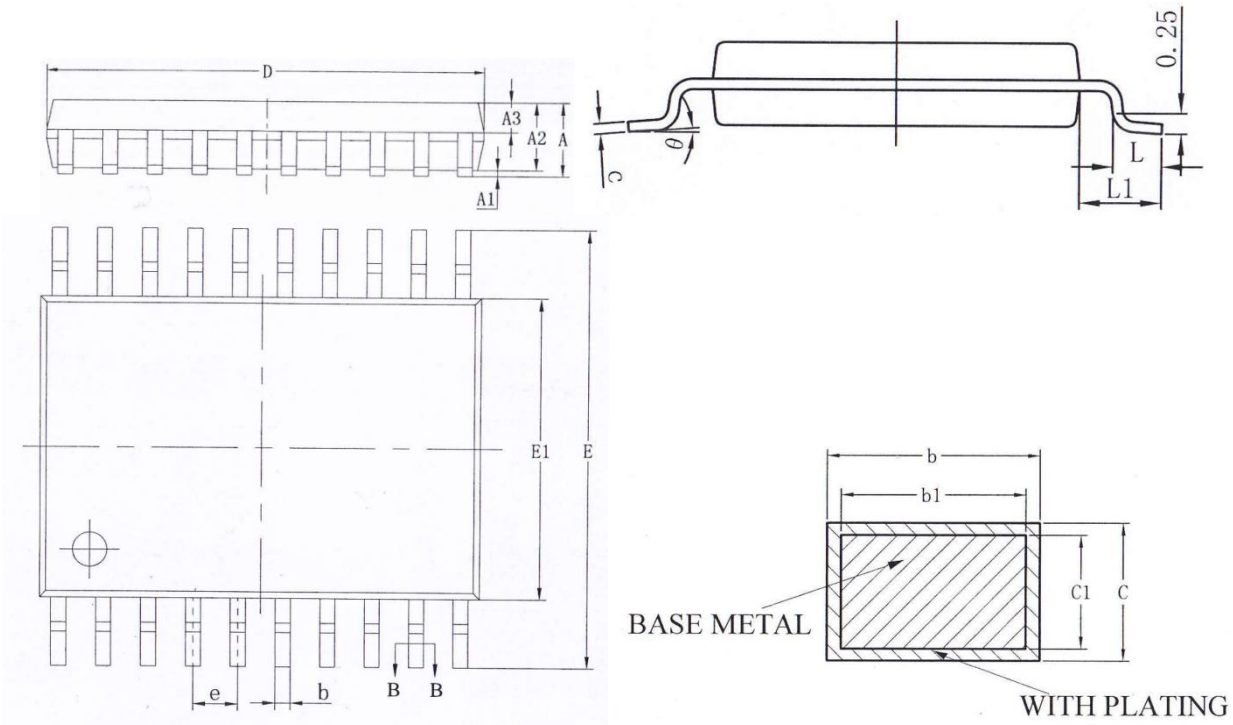


Figure10.HCSL Driver

PACKAGE DIMENSIONS(TSSOP-20)



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	8°

Reflow profile

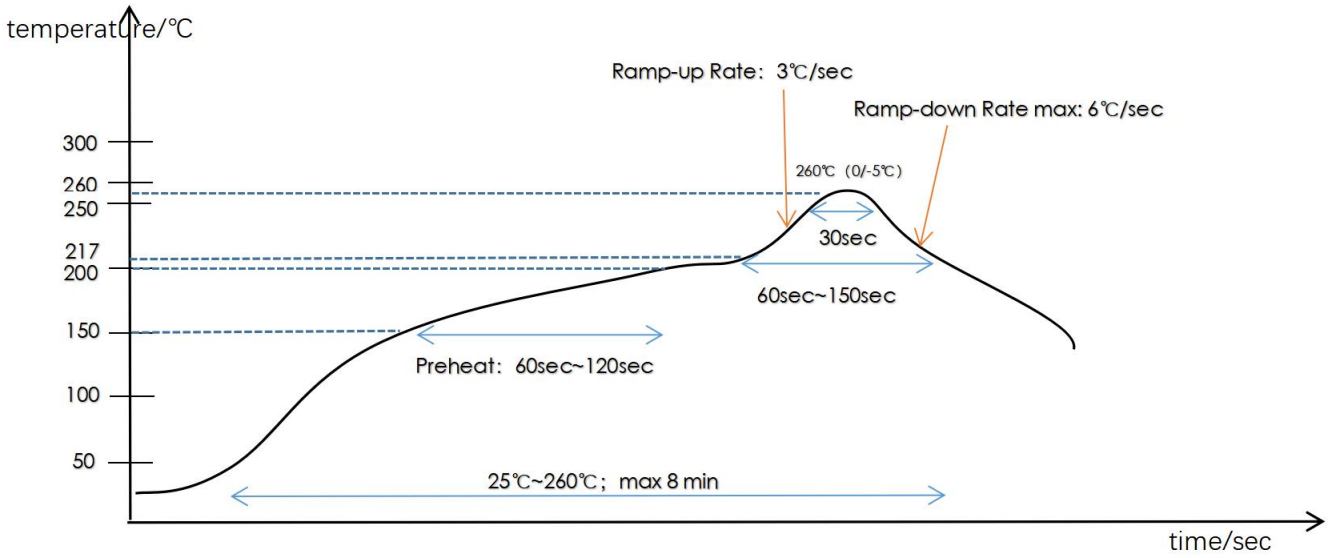


Figure11: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.03.27	First Draft.	1.0