US5S109 1.8V, 2.5V, 3.3V Low Skew LVCMOS Clock Buffer

Description

The US5S109 is a low skew, single input to nine output, clock buffer. Part of Ultrasilicon’ Clock family, this is a low skew, small clock buffer.

Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from -40℃ to 85℃.

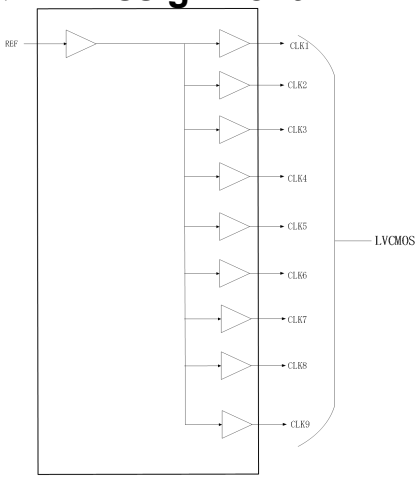
Features

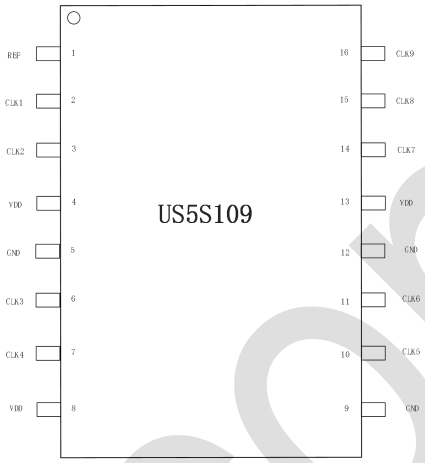
- High-Performance 1:9 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 50 ps (Typical)
- Very low propagation delay < 3 ns
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range: -40°C to 85°C
- Available in 16-Pin TSSOP Package

Device Information

Part Number	Package	Body Size(NOM)
US5S109	TSSOP-16	5.00mm x 4.40mm
US5S109S	SOP-16	9.90mm x 3.90mm

Block Diagram & Pin Assignment





Pin Descriptions and Function Table

Pin Number	Pin Name	Pin Type	Pin Description
1	REF	Input	Single-ended clock input with internal 150-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
2	CLK1	Output	LVCMOS Output 1, Typically connected to a receiver. Unused outputs can be left floating.
3	CLK2	Output	LVCMOS Output 2, Typically connected to a receiver. Unused outputs can be left floating.
4	VDD	Power	Connect to +1.8V, +2.5V, +3.3V .
5	GND	Power	Ground
6	CLK3	Output	LVCMOS Output 3, Typically connected to a receiver. Unused outputs can be left floating.
7	CLK4	Output	LVCMOS Output 4, Typically connected to a receiver. Unused outputs can be left floating.
8	VDD	Power	Connect to +1.8V, +2.5V, +3.3V .
9	GND	Power	Ground
10	CLK5	Output	LVCMOS Output 5, Typically connected to a receiver. Unused outputs can be left floating.
11	CLK6	Output	LVCMOS Output 6, Typically connected to a receiver. Unused outputs can be left floating.
12	GND	Power	Ground
13	VDD	Power	Connect to +1.8V, +2.5V, +3.3V .
14	CLK7	Output	LVCMOS Output 7, Typically connected to a receiver. Unused outputs can be left floating.
15	CLK8	Output	LVCMOS Output 8, Typically connected to a receiver. Unused outputs can be left floating.
16	CLK9	Output	LVCMOS Output 9, Typically connected to a receiver. Unused outputs can be left floating.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	4.6V
REF : Input voltage	-0.3V ~ VDD + 0.3V
T_J : Junction Temperature	150°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5% 1.8-5%	3.3 2.5 1.8	3.3+5% 2.5+5% 1.8+5%	V

DC Electrical Characteristics

VDD=1.8V ±5% , Ambient temperature -40℃ to +85℃, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, REF	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, REF	VIL				0.3*VDD	V
Input High Current, REF	IIH				30	uA
Input Low Current, REF	IIL				1	uA
Output High Voltage	VOH	IOH = -8 mA	1.2			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		15		mA

VDD=2.5V ±5%, Ambient temperature -40℃ to +85℃, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, REF	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, REF	VIL				0.3*VDD	V
Input High Current, REF	IIH				30	uA
Input Low Current, REF	IIL				1	uA
Output High Voltage	VOH	IOH = -8 mA	1.9			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		19		mA

VDD=3.3V ±5% , Ambient temperature -40℃ to +85℃, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Input High Voltage, REF	VIH	Nominal switching threshold is VDD/2	0.7*VDD		3.6	V
Input Low Voltage, REF	VIL				0.3*VDD	V
Input High Current, REF, OE	IIH				30	uA
Input Low Current, REF, OE	IIL				1	uA
Output High Voltage	VOH	IOH = -8 mA	2.6			V
Output Low Voltage	VOL	IOL = 8 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		24		mA

AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient Temperature -40℃ to +85℃, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		200	MHz
Output Rise Time	t_{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t_{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			2.0	4.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	$Jitter_{ADD}$	100MHz, 12KHz to 20MHz		55	85	fs

VDD = 2.5V ±5%, Ambient Temperature -40℃ to +85℃, unless stated otherwise

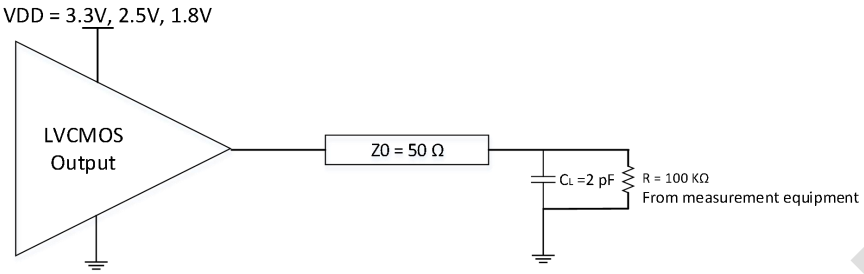
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		200	MHz
Output Rise Time	t_{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t_{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			1.5	3.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	$Jitter_{ADD}$	100MHz, 12KHz to 20MHz		25	45	fs

VDD = 3.3V ±5%, Ambient Temperature -40℃ to +85℃, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0.1		250	MHz
Output Rise Time	t_{OR}	20% to 80%		1.0	1.5	ns
Output Fall Time	t_{OF}	80% to 20%		1.0	1.5	ns
Propagation Delay	Note 1			1.0	2.0	ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps
Additive jitter	$Jitter_{ADD}$	100MHz, 12KHz to 20MHz		20	35	fs

Notes: 1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

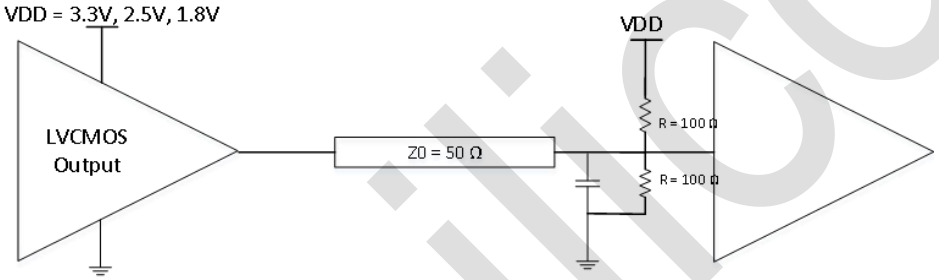
Parameter Measurement Information



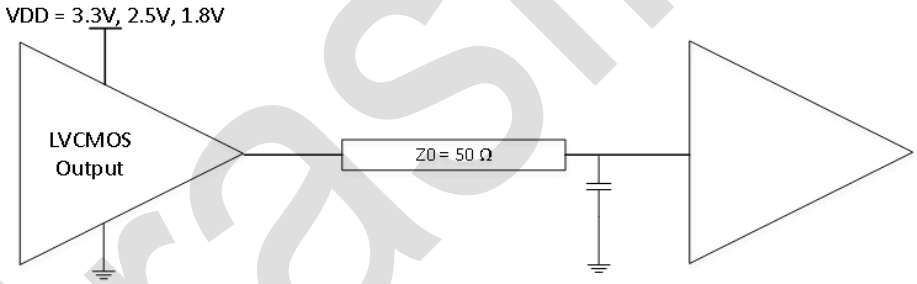
Test Load Circuit

Note:

1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency ≤ 250MHz, Z_O = 50 Ω, tr < 1.2ns, tf < 1.2ns.

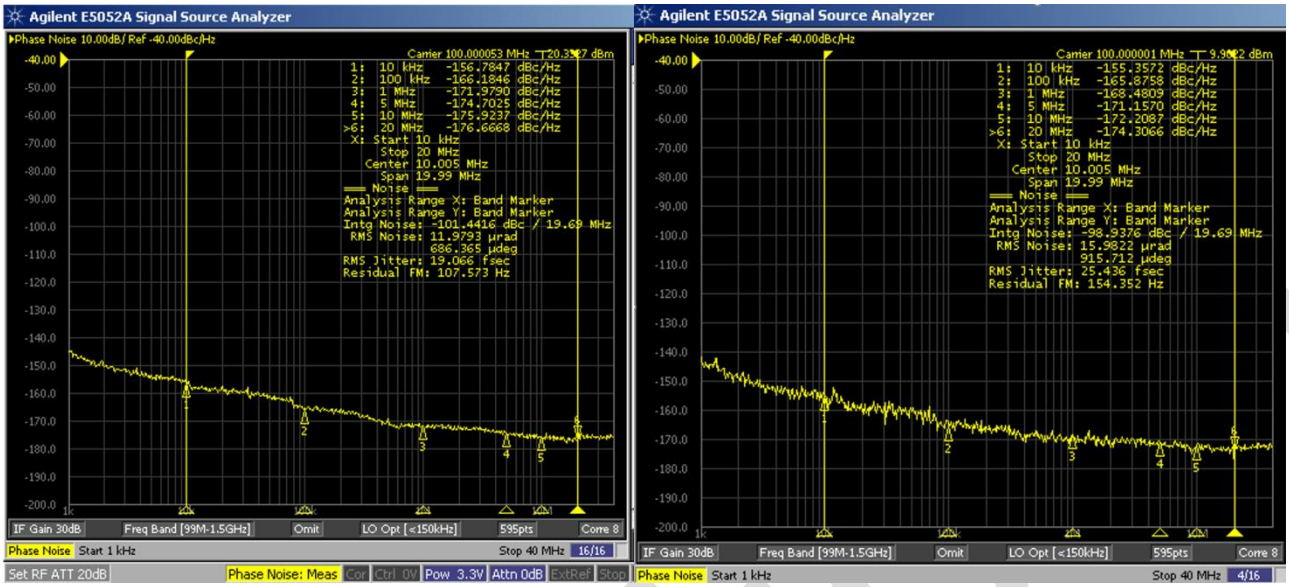


Application Load Witch 50-Ω Termination



Application Load With Termination

Phase Noise Plot

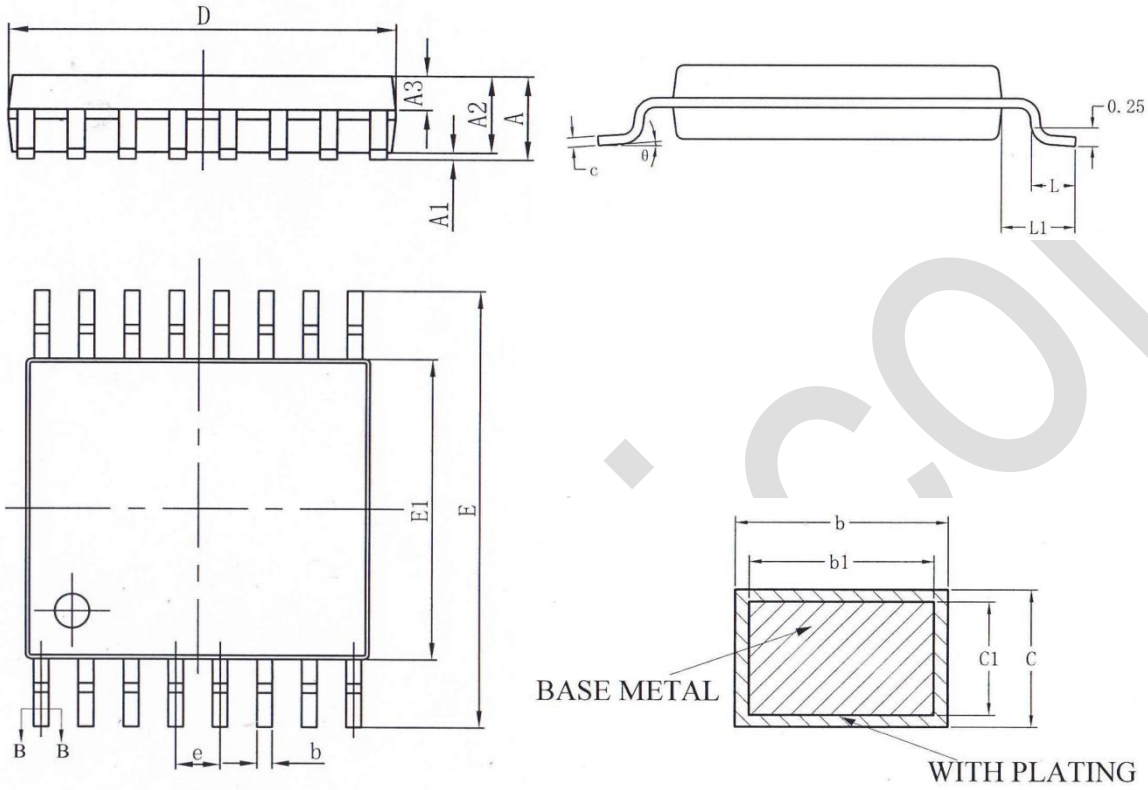


Wenzel 100MHz OCXO(19fs) Ouput Phase Noise(25.5fs)

The additive phase jitter for this device was measured using the Wenzel 100MHz OCXO(19fs) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

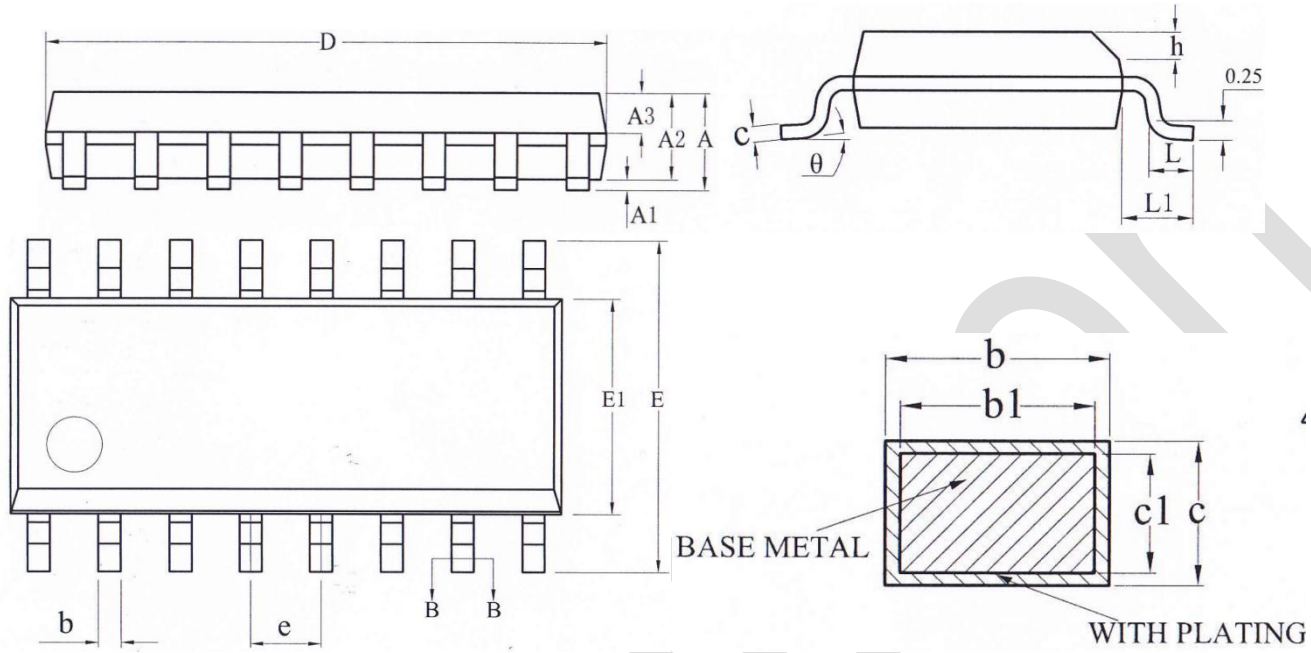
PACKAGE DIMENSIONS

1.TSSOP16



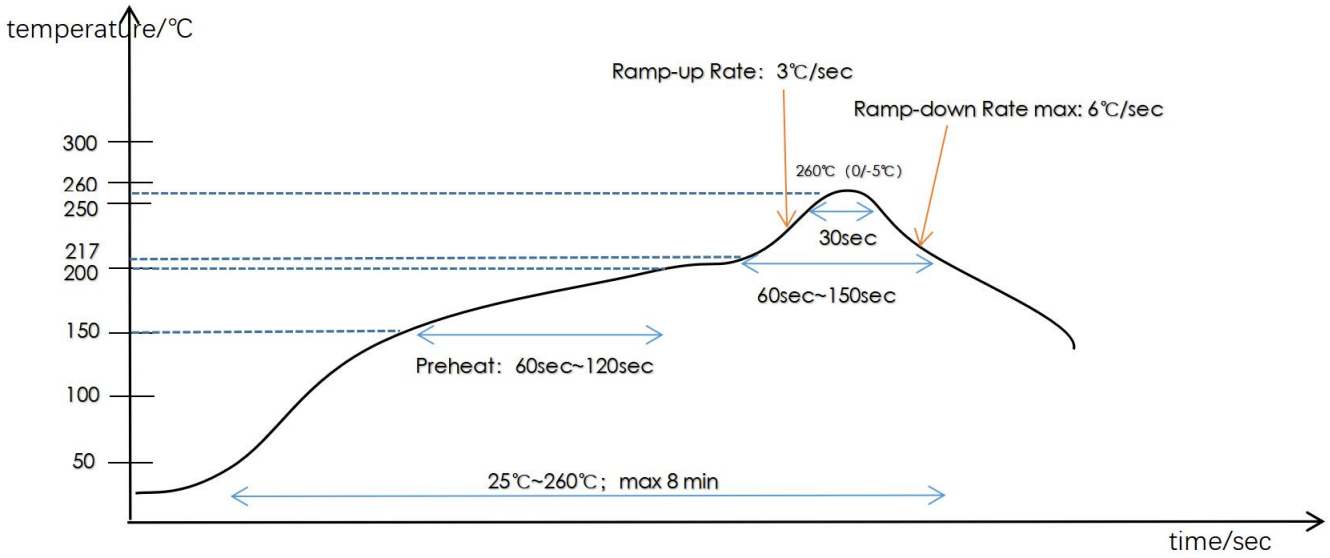
SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

2.SOP16



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E1	3.80	3.90	4.00
E	5.80	6.00	6.20
e	1.27BSC		
L	0.50	-	0.80
h	0.25	-	0.50
L1	1.05REF		
θ	0	-	8°

Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0
2022.06.11	ADD PACKAGE DIMENSIONS(SOP16).	2.0
2023.02.10	Operating frequency range change。	2.5