US5S102B 1.8V, 2.5V, 3.3V LVCMOS Clock Buffer

Description

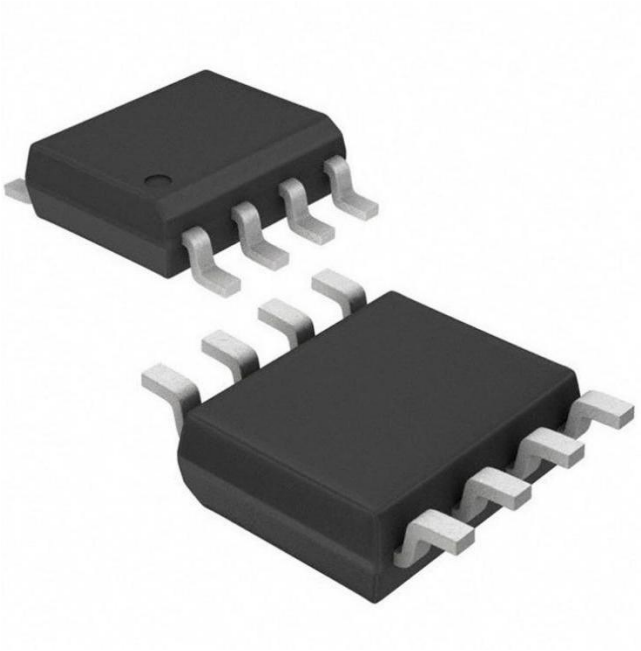
The US5S102B is a low skew, 1-to-2 Differential-to-LVCMOS Fanout Buffer and a member of High Performance Clock Solutions . The US5S102B has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTL input levels. The US5S102B features a pair of LVCMOS/LVTTL outputs. The US5S102B is characterized at full 3.3V for input VDD, and mixed 3.3V and 2.5V for output operating supply modes (VDDO). Guaranteed output and part-to-part skew characteristics make the US5S102B ideal for clock distribution applications demanding well defined performance and repeatibility.

Features

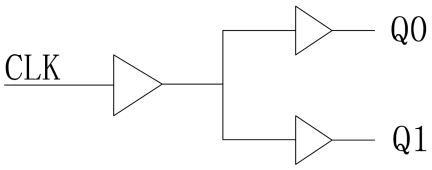
- 2 LVCMOS/LVTTL outputs
- LVCMOS/LVTTL clock input accepts LVCMOS or LVTTL input levels
- Output Skew : 25ps (Typical)
- Part-to-part skew: 250ps (maximum)
- FULL 3.3V,or 3.3V core,2.5V supply modes
- Maximum output frequency: 200MHz (typical)
- Industrial Temperature Range: -40°C to 85°C

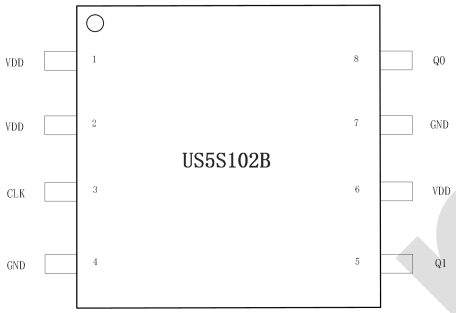
Device Information

Part Number	Package	Body Size(NOM)
US5S102B	SOP8	4.90mm x 6.00mm



Block Diagram





Pin Description and Function Table

Table 1: Pin Descriptions

Number	Name	Type		Description
1	VDD	Power		Output supply pin.
2	VDD	Power		Positive supply pin.
3	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
4	GND	Power		Power supply ground
5	Q1	Output		Clock output. LVCMOS / LVTTL interface levels.
6	VDD	Power		Output supply pin.
7	GND	Power		Power supply ground
8	Q0	Output		Clock output. LVCMOS / LVTTL interface levels.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	4.6V
V_{CLKIN} : Input voltage (CLKIN)	
V_{IN} : Input voltage (1G)	
V_{Yn} : Output pins (Yn)	-0.5V to V_{DD} + 0.5 V
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40	-	85	°C
T_J	Junction temperature		-	125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics

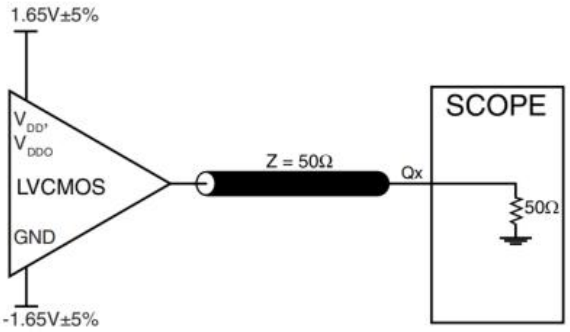
LVCMOS / LVTTL DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
VDD = 3.3V ± 5%, TA = -40°C TO 85°C						
VIH	Input High Voltage		0.7*VDD		VDD+0.3	V
VIL	Input Low Voltage				0.3*VDD	V
IIH	Input High Current/CLK	V_{DD} = V_{IN} =3.465V			150	μA
IIL	Input Low Current/CLK	V_{DD} = 3.465V,V_{IN} =0V	-5			μA
VOH	Output High Voltage	50Ω to 0.5VDD	2.6			V
		IOH = -100μA	2.9			V
VOL	Output Low Voltage	50Ω to 0.5VDD			0.5	V
		IOL = 100μA			0.2	V
VDD = 2.5V ± 5%, TA = -40°C TO 85°C						
VIH	Input High Voltage		0.7*VDD		VDD+0.3	V
VIL	Input Low Voltage				0.3*VDD	V
IIH	Input High Current/CLK				150	μA
IIL	Input Low Current/CLK		-5			μA
VOH	Output High Voltage	50Ω to 0.5VDD	1.8			V
		IOH = -100μA	2.2			V
VOL	Output Low Voltage	50Ω to 0.5VDD			0.5	V
		IOL = 100μA			0.2	V

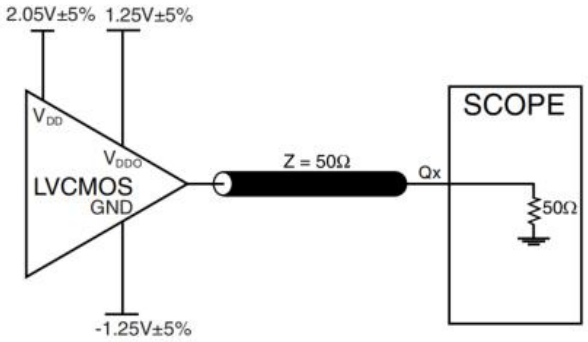
AC CHARACTERISTICS, VDD = 3.3V ± 5%, VDDO = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
VDD = 3.3V ± 5%, TA = -40°C TO 85°C						
fmax	Output Frequency		0.1		200	MHz
tPD	Propagation Delay	f≤200MHz	1.9	2.35	2.8	ns
tsk(o)	Output Skew			25	50	ps
tsk(pp)	Part-to-Part Skew			250	850	ps
tR	Output Rise Time	20% to 80%	300		800	ps
tF	Output Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle			50		%
VDD = 2.5V ± 5%, TA = -40°C TO 85°C						
fmax	Output Frequency		0.1		200	MHz
tPD	Propagation Delay	f≤350MHz	2.3		3.3	ns
tsk(o)	Output Skew			25	50	ps
tsk(pp)	Part-to-Part Skew			250	800	ps
tR	Output Rise Time	20% to 80%	250		650	ps
tF	Output Fall Time	20% to 80%	250		650	ps
odc	Output Duty Cycle			50		%

Parameter Measurement Information

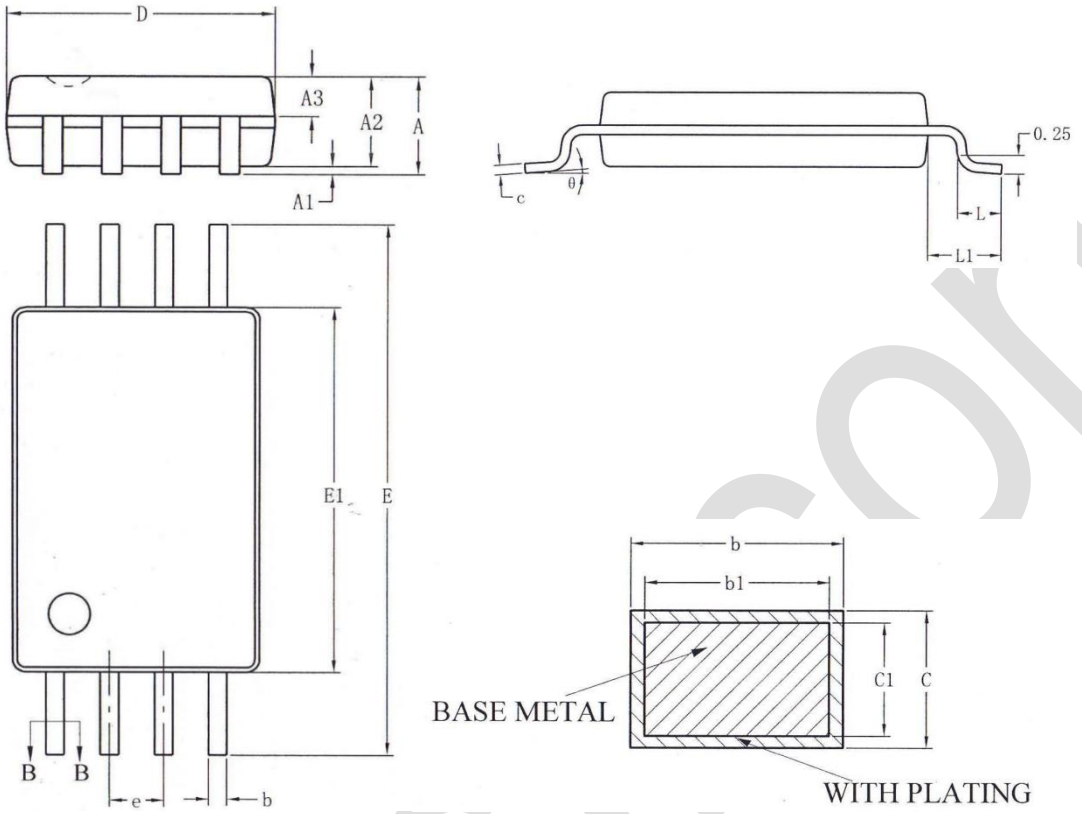


3.3V Output Load AC Test Circuit



3.3V/2.5V Output Load AC Test Circuit

PACKAGE DIMENSIONS



符号	单位（mm）		
	最小值	典型值	最大值
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 Basic		
h	0.25	-	0.50
L	0.50	-	0.80
θ	0°	-	8°

Reflow profile

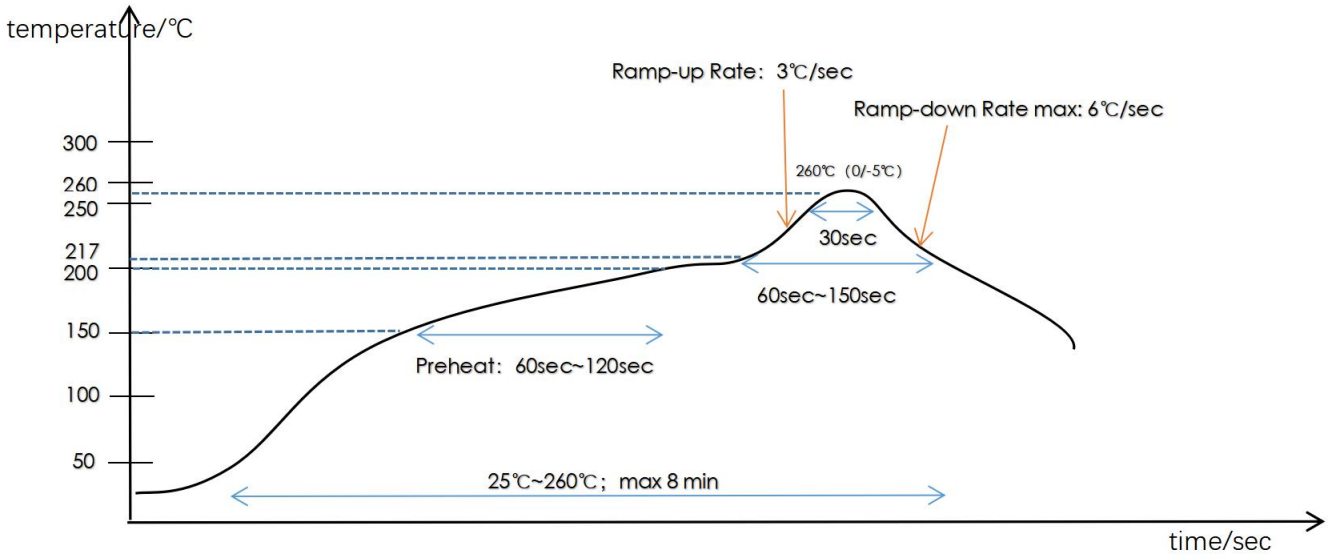


Figure1: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.09.28	First Draft.	1.0
2023.02.10	Operating frequency range change。	1.5