

Description

The US5S104, US5S106, US5S108, US5S110C, US5S112 is a modular high-performance, low-skew, general-purpose clock fanout buffer family. These clock buffers are designed with a modular approach in mind.

Five different fan-out variations, 1:4 to 1:12, are available. All of the devices are pin-compatible to each other for easy handling.

All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

All family members support an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from -40°C to 85°C .

Features

- High-Performance 1:10 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 55 ps (Typical)
- Very low propagation delay < 3 ns
- Synchronous Output Enable Is Available
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range: -40°C to 85°C
- Available in 20-Pin TSSOP Package

Applications

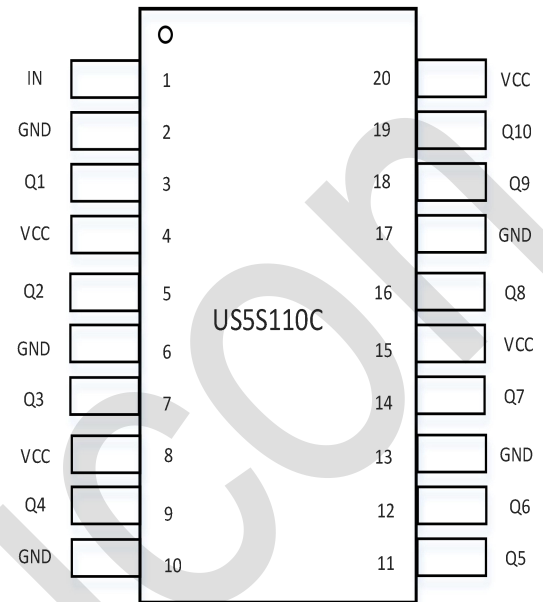
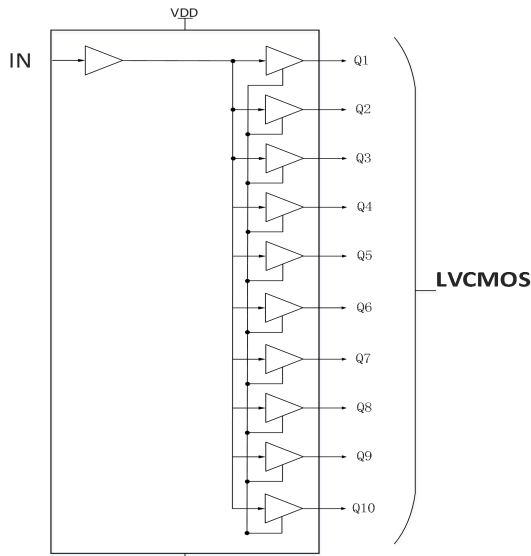
- General-Purpose Communication, Industrial, and Consumer Applications

Device Information

Part Number	Package	Body Size(NOM)
US5S110C	TSSOP-20	6.50mm x 4.40mm



Block Diagram



Pin Description and Function Table

Table 1: Pin Descriptions

Number	Name	Type	Description
1	IN	Input	Single-ended clock input with internal 150-k Ω (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
2	GND	Power	Ground.
3	Q1	Output	LVC MOS output 1. Typically connected to a receiver. Unused outputs can be left floating.
4	VCC	Power	DC power supply, 1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1- μ F capacitor near the pin.
5	Q2	Output	LVC MOS output 2. Typically connected to a receiver. Unused outputs can be left floating.
6	GND	Power	Ground.
7	Q3	Output	LVC MOS output 3. Typically connected to a receiver. Unused outputs can be left floating.
8	VCC	Power	DC power supply, 1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1- μ F capacitor near the pin.
9	Q4	Output	LVC MOS output 4. Typically connected to a receiver. Unused outputs can be left floating.
10	GND	Power	Ground.
11	Q5	Output	LVC MOS output 5. Typically connected to a receiver. Unused outputs can be left floating.
12	Q6	Output	LVC MOS output 6. Typically connected to a receiver. Unused outputs can be left floating.
13	GND	Power	Ground.
14	Q7	Output	LVC MOS output 7. Typically connected to a receiver. Unused outputs can be left floating.
15	VCC	Power	DC power supply, 1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1- μ F capacitor near the pin.

Number	Name	Type	Description
16	Q8	Output	LVC MOS output 8. Typically connected to a receiver. Unused outputs can be left floating.
17	GND	Power	Ground.
18	Q9	Output	LVC MOS output 9. Typically connected to a receiver. Unused outputs can be left floating.
19	Q10	Output	LVC MOS output 10. Typically connected to a receiver. Unused outputs can be left floating.
20	VCC	Power	DC power supply, 1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1- μ F capacitor near the pin.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
V _{DD} : Supply voltage	0.5V to 3.6V
V _{CLKIN} : Input voltage (CLKIN)	
V _{Yn} : Output pins (Qn)	-0.5V to V _{DD} + 0.3 V
T _{STG} : Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T _A	Ambient air temperature	-40	-	85	°C
T _J	Junction temperature		-	125	°C
V _{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	
		1.8-5%	1.8	1.8+5%	

Electrical Characteristics

VDD = 3.3 V ± 5 %, -40°C ≤ T_A ≤ 85°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Core supply current	All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 1.8 V		11		mA
		All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 2.5 V		16		
		All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 3.3 V		22		
CLOCK INPUT						
f _{IN_SE}	Input frequency	V _{DD} = 3.3 V	0.1		250	MHz
		V _{DD} = 2.5 V and 1.8 V	0.1		200	
V _{IH}	Input high voltage		0.7 x V _{DD}			V
V _{IL}	Input low voltage				0.3 x V _{DD}	
dV _{IN} /dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I _{IN_LEAK}	Input leakage current		-50		50	uA
C _{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V _{DD} LEVELS						
f _{OUT}	Output frequency	V _{DD} = 3.3 V	0.1		250	MHz
		V _{DD} = 2.5 V and 1.8 V	0.1		200	
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t _{START}	Start-up time before output is active	See (1)			3	ms
t _{1G_ON}	Output enable time	See (2)			5	cycles
t _{1G_OFF}	Output disable time	See (3)			5	cycles
CLOCK OUTPUT FOR V _{DD} = 3.3 V ± 5%						
V _{OH}	Output high voltage	I _{OH} = -8 mA	2.6			V
V _{OL}	Output low voltage	I _{OL} = 8 mA			0.5	
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25 MHz		0.35	0.7	ns
t _{OUTPUT-SKEW}	Output-output skew	See (4)		25	50	ps
t _{PART-SKEW}	Part-to-part skew				450	
t _{PROPDELAY}	Propagation delay	See (5)		1.5	2	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		20	35	fs, RMS
R _{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V _{DD} = 2.5 V ± 5%						
V _{OH}	Output high voltage	I _{OH} = -8 mA	1.9			V
V _{OL}	Output low voltage	I _{OL} = 8 mA			0.5	
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25 MHz		0.33	0.8	ns
t _{OUTPUT-SKEW}	Output-output skew	See (4)			50	ps
t _{PART-SKEW}	Part-to-part skew				400	
t _{PROP-DELAY}	Propagation delay	See (5)		1.5	2.5	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		25	45	fs, RMS
R _{OUT}	Output impedance			50		Ω

- (1) Measured from VDD stable to output active, when 1G = HIGH.
- (2) Measured from 1G rising edge crossing V_{IH} to first rising edge of Y_n.
- (3) Measured from 1G falling edge crossing V_{IL} to last falling edge of Y_n.
- (4) Measured from rising edge of any Y_n output to any other Y_m output.
- (5) Measured from rising edge of CLKIN to any Y_n output.

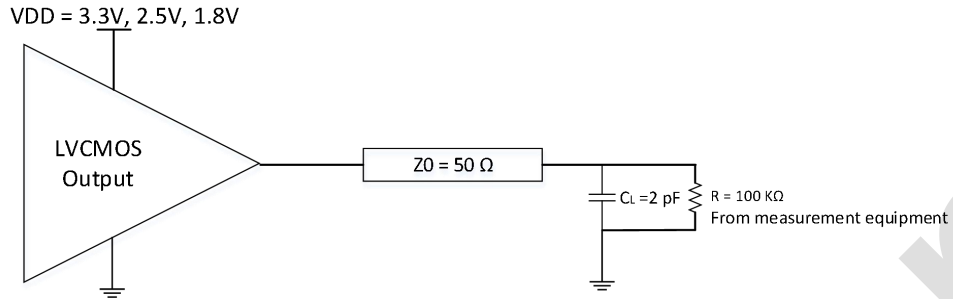
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT FOR $V_{DD} = 1.8\text{ V} \pm 5\%$						
V_{OH}	Output high voltage	$I_{OH} = -8\text{ mA}$	2.6			V
V_{OL}	Output low voltage	$I_{OL} = 8\text{ mA}$			0.5	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, $C_L = 5\text{ pF}$, $f_{IN} = 156.25\text{ MHz}$		0.38	1	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (4)			50	ps
$t_{PART-SKEW}$	Part-to-part skew				900	ps
$t_{PROP-DELAY}$	Propagation delay	See (5)		1.5	3	ns
$t_{JITTER-ADD}$	Additive Jitter	$f_{IN} = 100\text{ MHz}$, Input slew rate = 2 V/ns , Integration range = $12\text{ kHz} - 20\text{ MHz}$		55	85	fs, RMS
R_{OUT}	Output impedance			50		Ω
Power dissipation capacitance per output						
Cpd		$V_{DD} = 3.3\text{ V}$; $f = 10\text{ MHz}$			9.5	pF
		$V_{DD} = 2.5\text{ V}$; $f = 10\text{ MHz}$			9.4	
		$V_{DD} = 1.8\text{ V}$; $f = 10\text{ MHz}$			9.4	

Timing Requirements

$V_{DD} = 3.3\text{ V} \pm 5\%$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

Power Supply		Min	Typ	Max	Unit
V/t_{RAMP}	V_{DD} ramp rate	0.1	-	50	V/rms

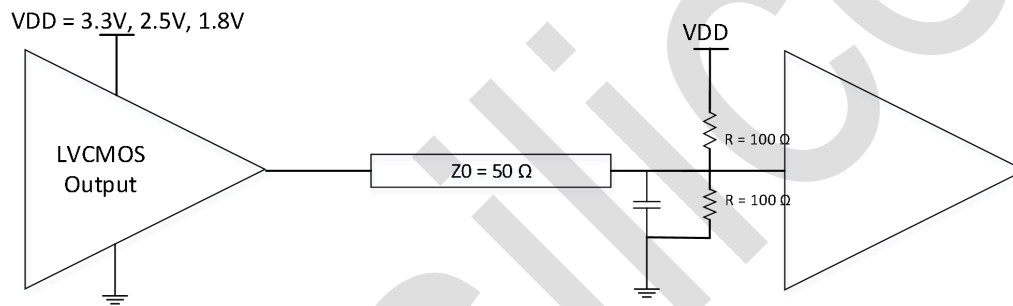
Parameter Measurement Information



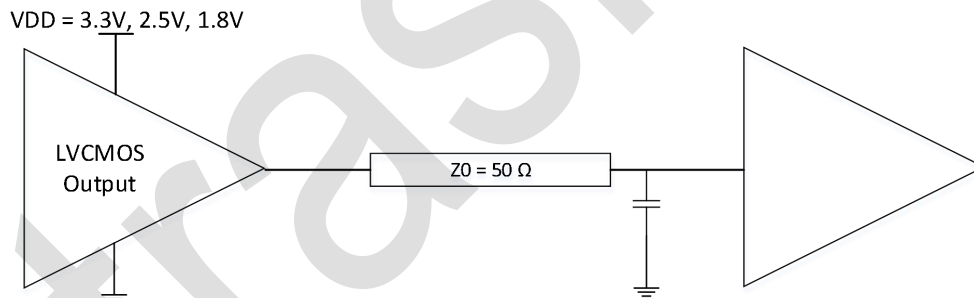
Test Load Circuit

Note:

1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency $\leq 250\text{MHz}$, $Z_0 = 50 \Omega$, $t_r < 1.2\text{ns}$, $t_f < 1.2\text{ns}$

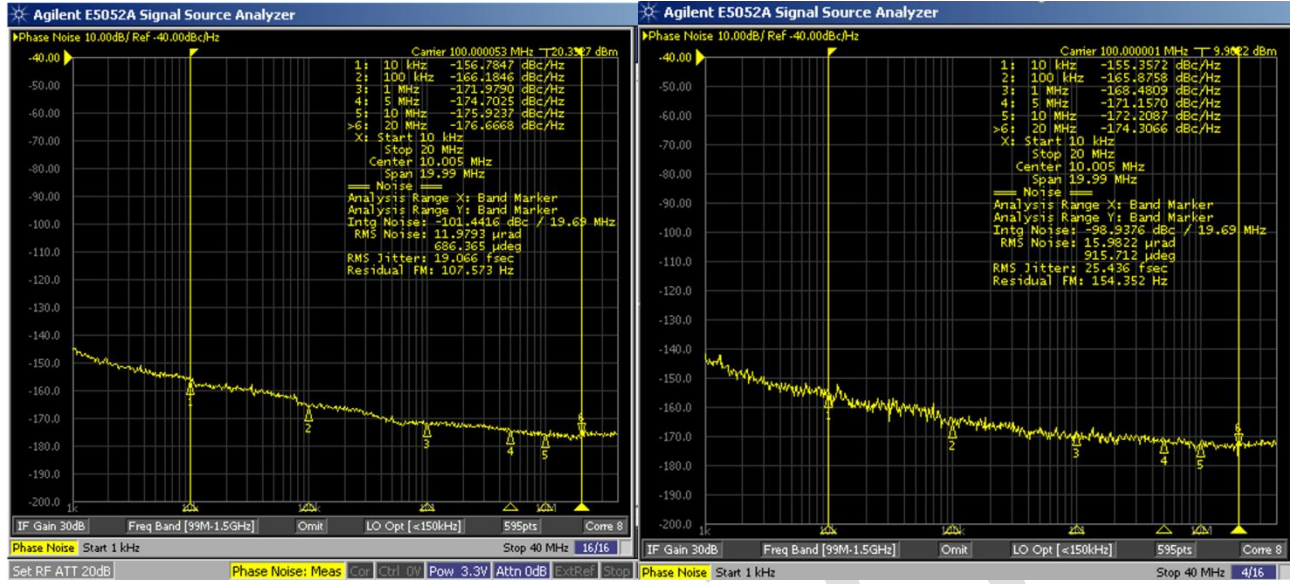


Application Load Witch 50-Ω Termination



Application Load With Termination

Phase Noise Plot

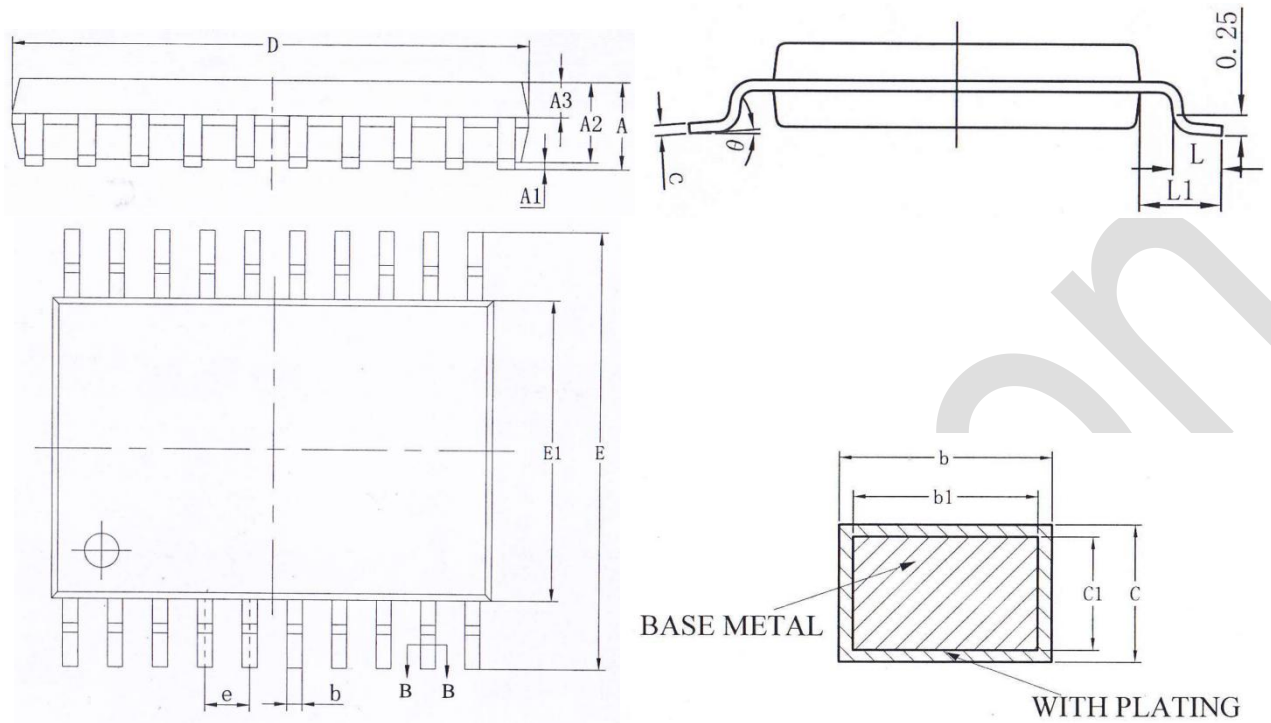


Wenzel 100MHz OCXO(19fs)

Output Phase Noise(25.5fs)

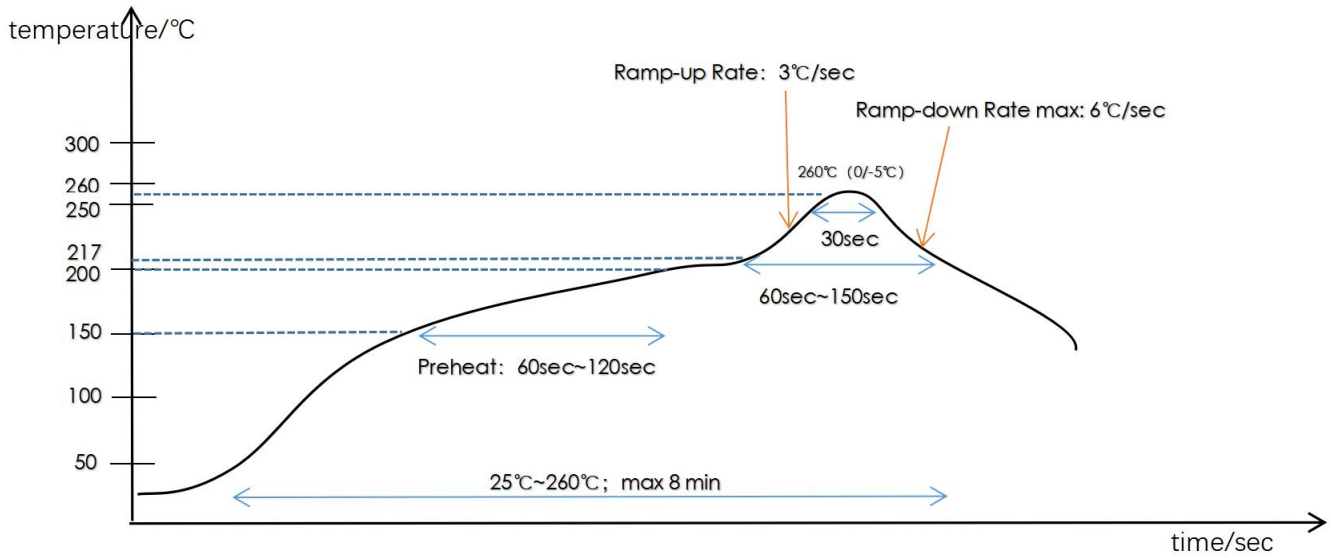
The additive phase jitter for this device was measured using the Wenzel 100MHz OCXO(19fs) as an input source with an Agilent E5052A phase noise analyzer. (VDD=3.3V)

PACKAGE DIMENSIONS



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	8°

Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.08.10	First Draft.	1.0
2023.02.10	Operating frequency range change.	1.5

Ultrasilicon