US5S204 1.8V, 2.5V, 3.3V LVCMOS Clock Buffer

Description

US5S204 is a widely used, low-jitter, low-power clock sector output buffer. It can allocate one of two inputs to four low-jitter LVCMOS clock outputs. Its can adopt differential or single-ended signals inputs. This buffer is suitable for various mobile and wired infrastructure, data communication, computing, low-power medical imaging and portable test and measurement applications. The core voltage of the device supports 2.5 V or 3.3 V, and the output voltage supports 1.5 V, 1.8 V, 2.5 V or 3.3 V.

Applications

- General-Purpose Communication, Industrial, and Consumer Applications

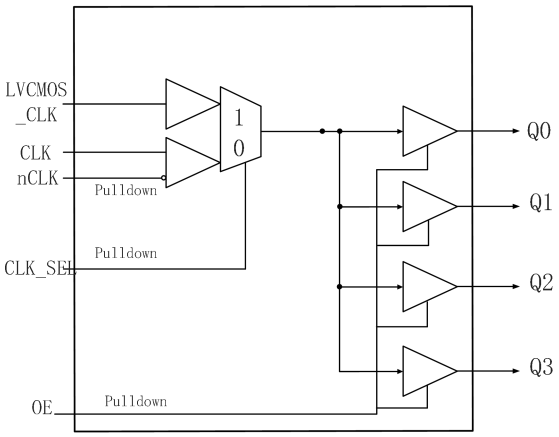
Device Information

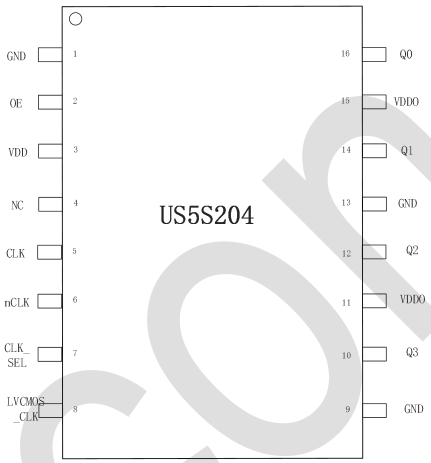
Part Number	Package	Body Size(NOM)
US5S204	TSSOP-16	5.00mm x 4.40mm

Features

- High-Performance 2:4 LVCMOS Clock Buffer
- Output Skew < 50 ps (Typical3.3V)
- Transmission delay : 1.5 ns (Typical)
- Maximum operating frequency : 250MHz(VDDO=3.3V)
- Input supports LVPECL, LVDS, HCSL, SSTL or LVCMOS signal
- Differential and single terminal support 250MHz
- Supply voltage(VDD/VDDO):
  3.3V/3.3V, 2.5V,1.8V,1.5V
  2.5V/2.5V,1.8V,1.5V
- Additive RMS phase jitter @ 156.25MHz:
  ＜100 fs RMS (10kHz - 20MHz)
- Industrial Temperature Range: -40°C to 85°C
- Available in 16-Pin TSSOP Package

Block Diagram





Pin Description and Function Table

管脚号	管脚名称	管脚类型	说明
1	GND	Power	Ground.
2	OE	Input	Output enable input. 0 = Outputs in Hi-Z state 1 = Outputs in active state.
3	VDD	Power	Power supply.
4	NC	NC	NC.
5	CLK	Input	Non-inverting differential clock input 0.
6	nCLK	Input	Inverting differential clock input 0. Internally biased to VDD/2 when left floating.
7	CLK_SEL	Input	Clock select input. 0 = Select CLK, nCLK 1 = Select LVCMOS_CLK.
8	LVCMOS_CLK	Input	Single-ended clock input.
9	GND	Power	Ground.
10	Q3	Output	Single-ended clock outputs 3.
11	VDDO	Power	Output supply pin.
12	Q2	Output	Single-ended clock outputs 2.
13	GND	Power	Ground.
14	Q1	Output	Single-ended clock outputs 1.
15	VDDO	Power	Output supply pin.
16	Q0	Output	Single-ended clock outputs 0.

Input logic

CLK_SEL	输入选择
0	CLK,nCLK
1	LVCMOS_CLK

OE Control Table

OE	Qx
0	Hiz
1	Enable

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	-0.5V to 4.6V
V_{IN} : Input voltage	-0.5V to V_{DD} + 0.5 V
V_{OUT} : Output voltage	
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

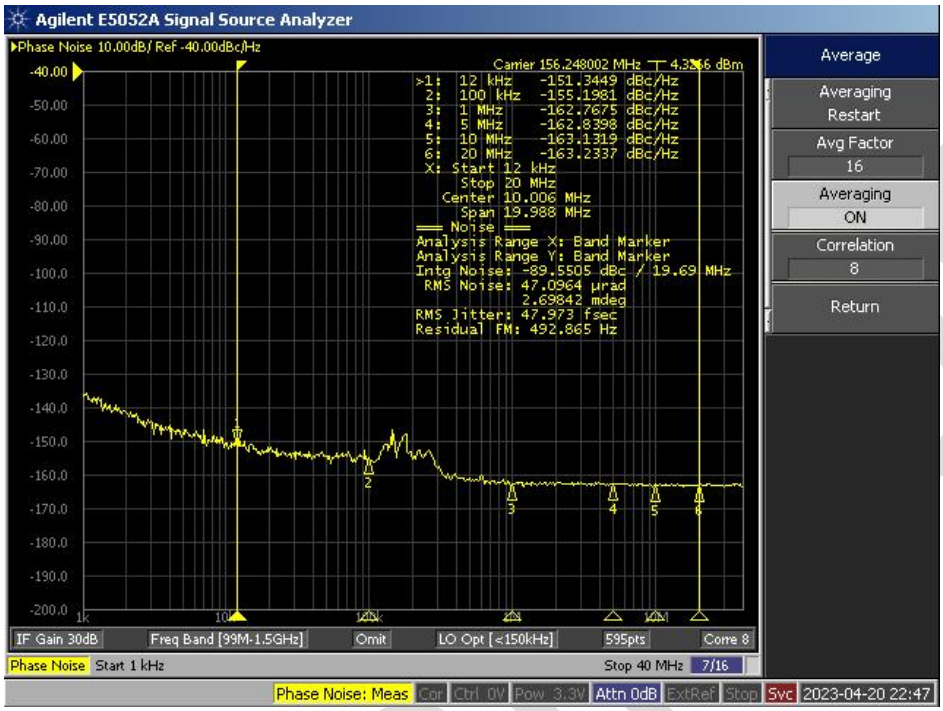
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40	-	85	°C
T_J	Junction temperature		-	125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V
V_{DDO}	output voltage	3.3-5% 2.5-5% 1.8-5% 1.5-5%	3.3 2.5 1.8 1.5	3.3+5% 2.5+5% 1.8+5% 1.5+5%	V

Electrical Characteristics

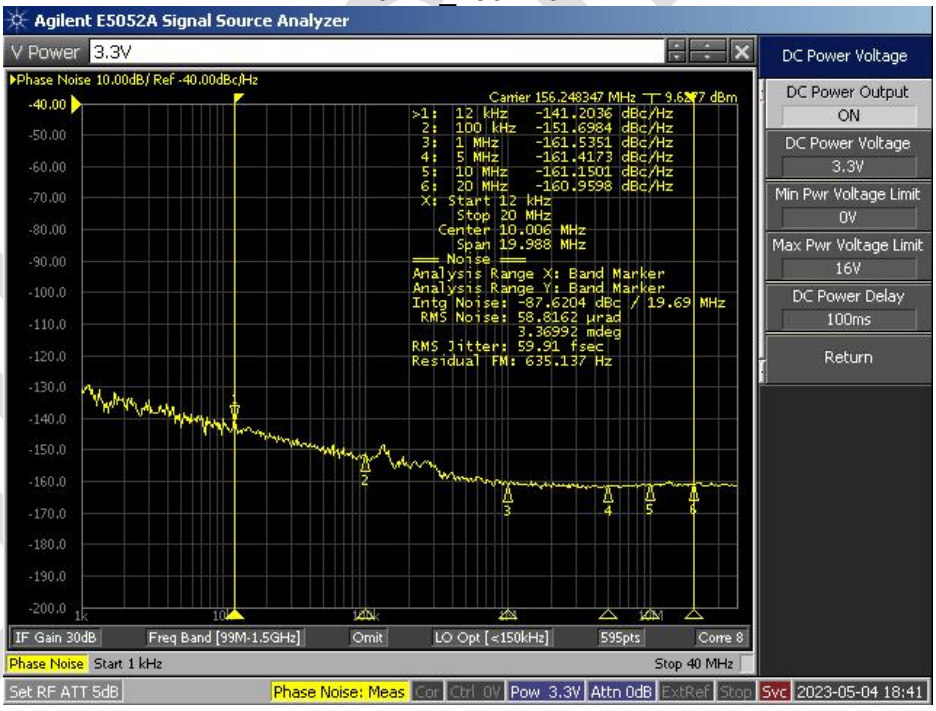
VDD = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 85°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input characteristics						
INPUT						
I_{DD_LVCMOS}	Core supply current	Power Supply Current through VDD, VDDO,10MHz		8.6		mA
$I_{DD\_Differential}$	Core supply current	Power Supply Current through VDD, VDDO,10MHz		9.3		mA
f_{CLKin}	Input frequency		0.1		250	MHz
V_{IHD}	Input high voltage	Differential input			VDD	V
V_{ILD}	Input low voltage		GND			V
V_{ID}	Differential input voltage swing		0.15		1.3	V
V_{CMD}	Differential input common mode voltage		0.5		VDD – 0.85	V
V_{IH}	Single-ended input high-level voltage	Single-ended input (DC or AC coupling)			VDD	V
V_{IL}	Single-end input low-level voltage		GND			V
V_{I_SE}	Single-end input voltage swing		0.3		2	V
V_{CM}	Single-ended input common mode voltage		0.25		VDD - 1.2	V
LVCMOS output characteristics						
f_{OUT}	Maximum output frequency		0.1		250	MHz
$Jitter_{ADD}$	Additional jitter (12KHz-20MHz)	CLKin: 156.25 MHz,LVCMOS Input		65		fs
		CLKin: 156.25 MHz,Differential Input		36		
Duty Cycle	Duty Cycle		45%		55%	
V_{OH}	High voltage output	I_{OH} = -8 mA	2.6			V
V_{OL}	Low voltage output	I_{OH} = 8 mA			0.5	V
t_R	Output rise time （20% TO 80% ）			0.32	0.8	ns
t_F	Output drop time （80% TO 20%）			0.32	0.8	ns
Transmission delay and output skew						
t_{PD}	Propagation delay			1.5	2	ns
$t_{SK(O)}$	output skew			9.2	50	ps
$t_{PART-SKEW}$	Part-to-part skew				400	ps

PHASE JITTER

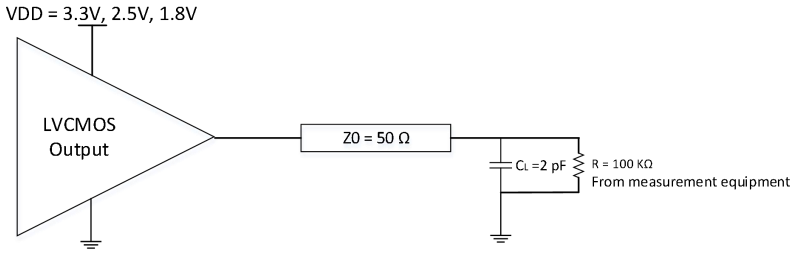


Jitter_156M25



Jitter_3V3_differential_Input

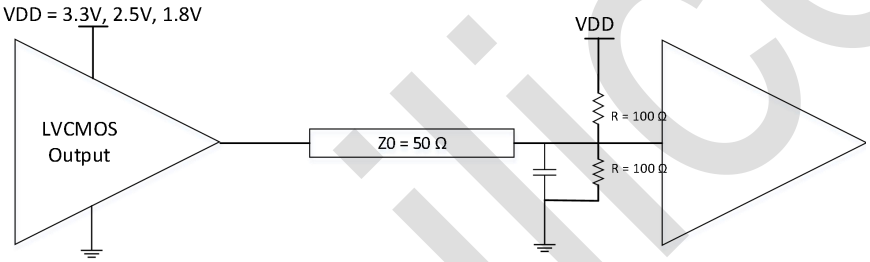
Parameter Measurement Information



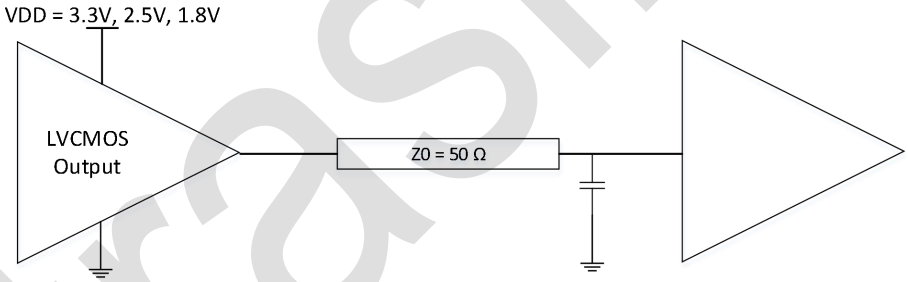
Test Load Circuit

Note:

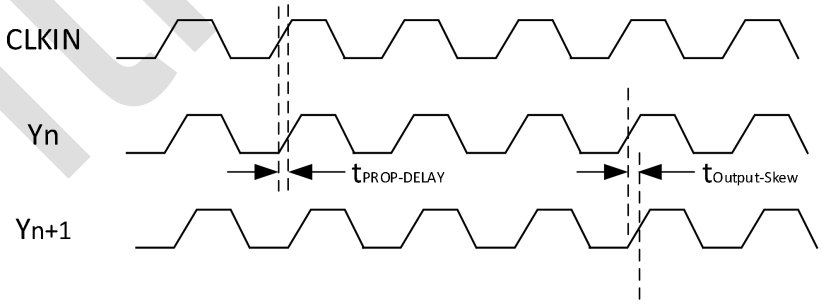
1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency ≤ 250MHz, Z_O = 50 Ω, tr < 1.2ns, tf < 1.2ns



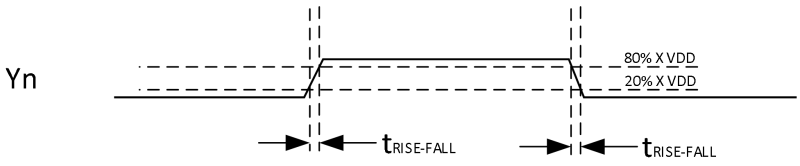
Application Load Witch 50-Ω Termination



Application Load With Termination

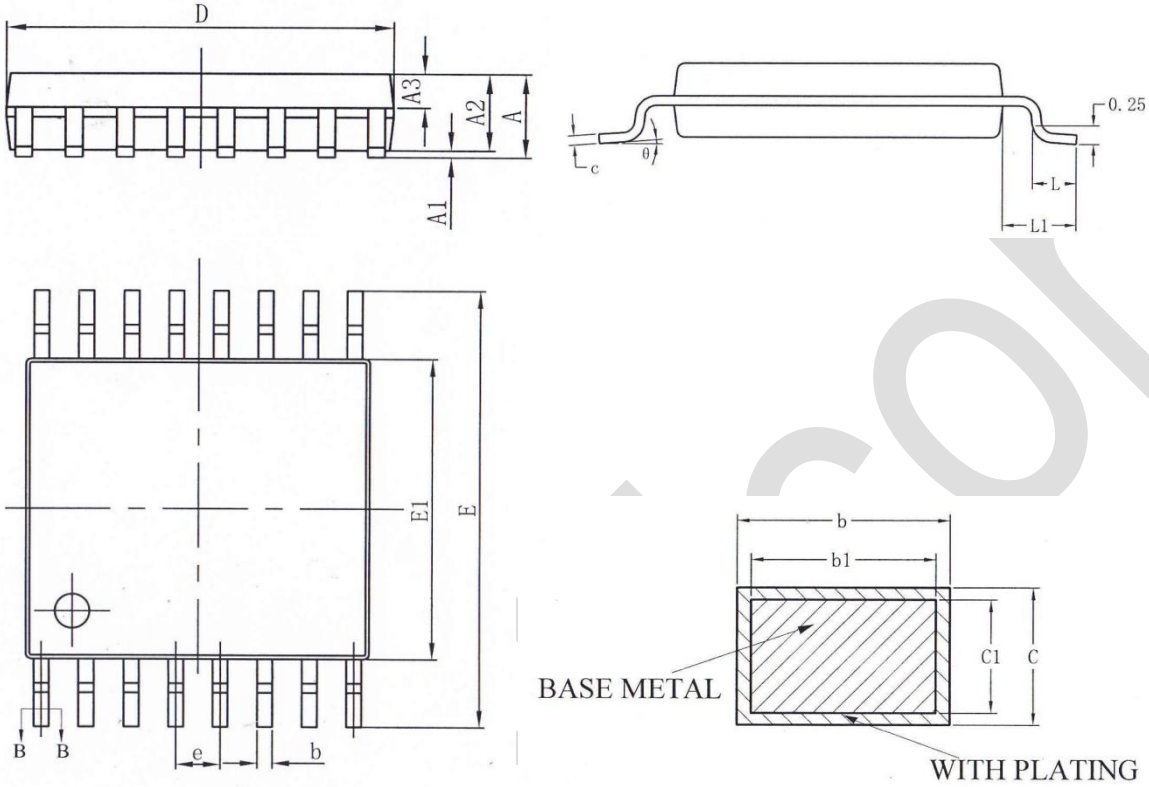


Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$



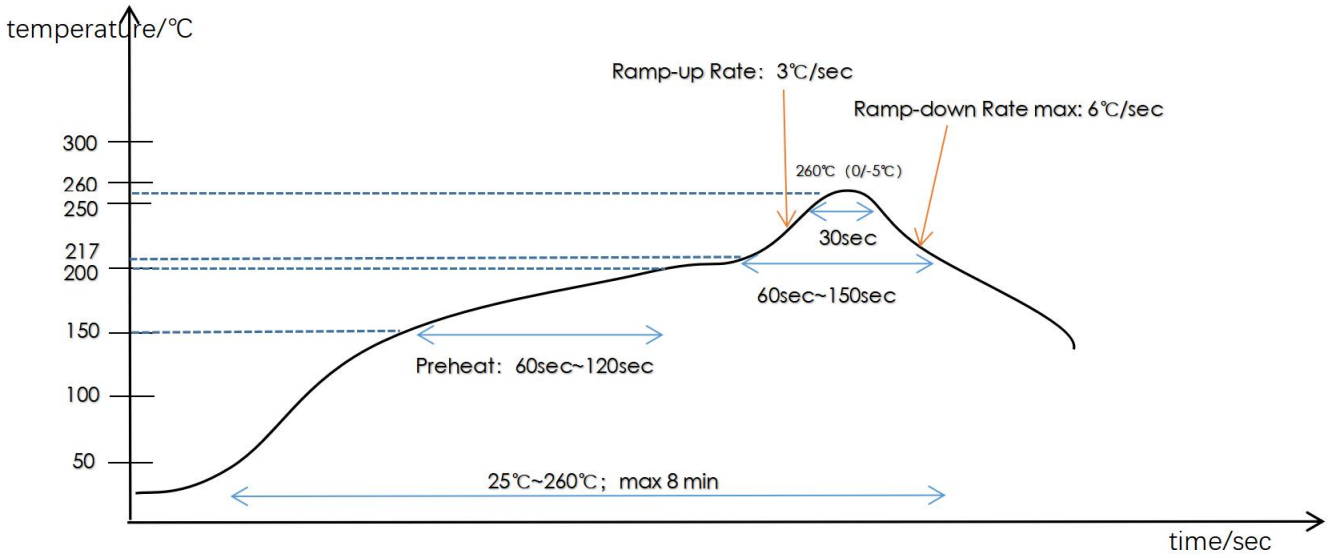
Rise and Fall Time $t_{RISE-FAIL}$

PACKAGE DIMENSIONS



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.05.05	First Draft.	1.0