

## Description

The US5D338 is a 400MHz, 8-output differential high-performance 8-output PCIe Gen1/Gen2/Gen3/Gen4/Gen5 fanout buffer.

The input clock can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 4 HCSL outputs and one LVCMOS output. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The outputs are at a defined level when inputs are open.

The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock.

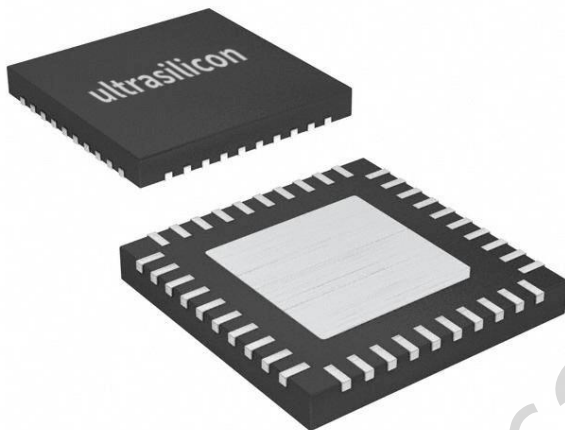
The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V core power supply, and either a 3.3V or 2.5V output operating supply.

## Applications

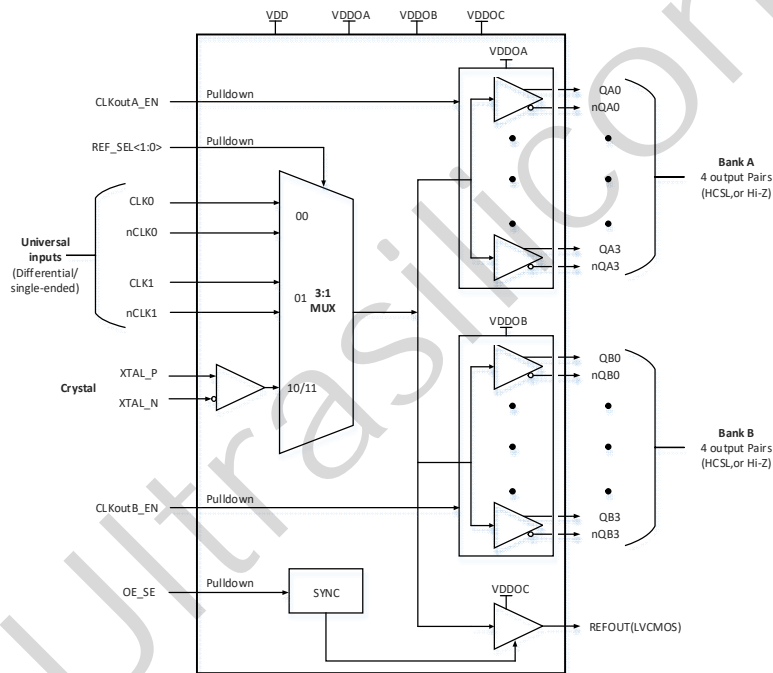
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH, CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express (PCIe 3.0, 4.0, 5.0)
- Remote Radio Units and Baseband Units

## Features

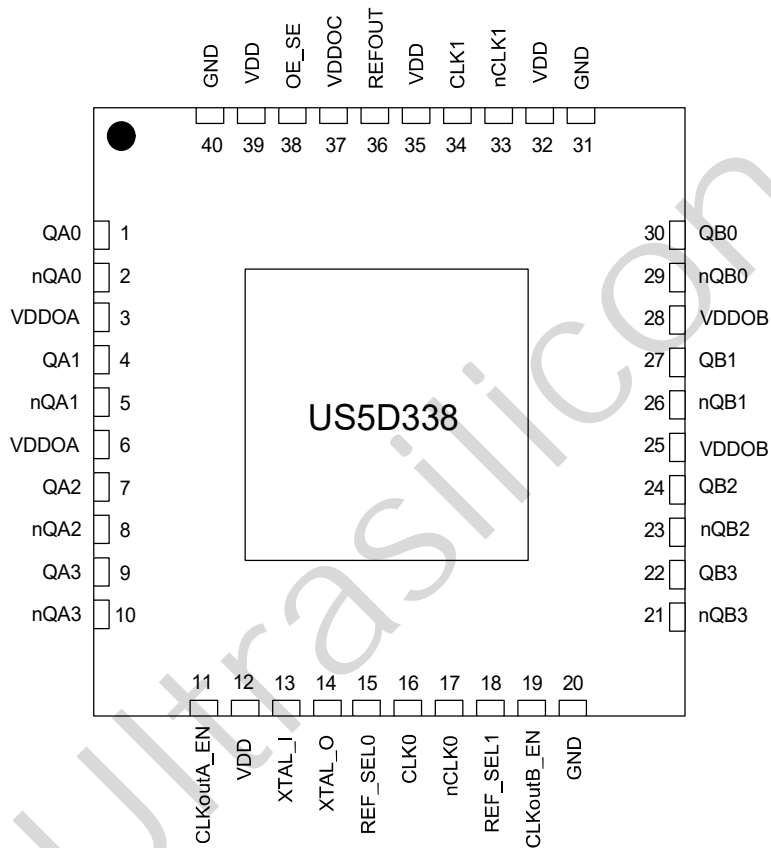
- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Crystal Input accepts 10MHz to 48MHz Crystal or Single Ended Clock
- Maximum Output Frequency
  - HCSL - 400MHz
  - LVCMOS - 250MHz
- Two banks, each has four differential output pairs
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 20ps (typical)  
(Bank A and Bank B at the same output level)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter @ 156.25MHz:  
70fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage modes:
  - $V_{DD}/V_{DDO}$   
3.3V/3.3V
  - 3.3V/2.5V
- Industrial Temperature Range: -40°C to 85°C
- Available in a 40-pin, 6mm\*6mm WQFN package



## Block Diagram



Pin Assignment for 6mm x 6mm 40-Lead WQFN Package



## Pin Description and Pin Characteristic Tables

**Table 1: Pin Descriptions<sup>1</sup>**

Number	Name	Type	Description
1	QA0	Output	Differential Bank A clock output pair. HCSL interface levels.
2	nQA0	Output	Differential Bank A clock output pair. HCSL interface levels.
3	V <sub>DDOA</sub>	Power	Output supply pins for Bank QA outputs. 3.3V or 2.5V.
4	QA1	Output	Differential Bank A clock output pair. HCSL interface levels.
5	nQA1	Output	Differential Bank A clock output pair. HCSL interface levels.
6	V <sub>DDOA</sub>	Power	Output supply pins for Bank QA outputs. 3.3V or 2.5V.
7	QA2	Output	Differential Bank A clock output pair. HCSL interface levels.
8	nQA2	Output	Differential Bank A clock output pair. HCSL interface levels.
9	QA3	Output	Differential Bank A clock output pair. HCSL interface levels.
10	nQA3	Output	Differential Bank A clock output pair. HCSL interface levels.
11	CLKoutA_EN	Input	Pulldown Output driver select for Bank A outputs.
12	V <sub>DD</sub>	Power	Power supply for Core and input Buffer blocks, 3.3V.
13	XTAL_I	Input	Crystal oscillator interface.
14	XTAL_O	Input	Crystal oscillator interface.
15	REF_SEL0	Input	Pulldown Input clock selection.
16	CLK0	Input	Pulldown Non-inverting differential clock. Internally biased to ground.
17	nCLK0	Input	Pullup/ Pulldown Inverting differential clock. Internally biased to 0.5V <sub>DD</sub> .
18	REF_SEL1	Input	Pulldown Input clock selection.
19	CLKoutB_EN	Input	Pulldown Output driver select for Bank B outputs.
20	GND	Power	Ground.
21	nQB3	Output	Differential Bank B clock output pair. HCSL interface levels.
22	QB3	Output	Differential Bank B clock output pair. HCSL interface levels.
23	nQB2	Output	Differential Bank B clock output pair. HCSL interface levels.
24	QB2	Output	Differential Bank B clock output pair. HCSL interface levels.
25	V <sub>DDOB</sub>	Power	Output supply pins for Bank QB outputs. 3.3V or 2.5V.
26	nQB1	Output	Differential Bank B clock output pair. HCSL interface levels.
27	QB1	Output	Differential Bank B clock output pair. HCSL interface levels.
28	V <sub>DDOB</sub>	Power	Output supply pins for Bank QB outputs. 3.3V or 2.5V.
29	nQB0	Output	Differential Bank B clock output pair. HCSL interface levels.
30	QB0	Output	Differential Bank B clock output pair. HCSL interface levels.
31	GND	Power	Ground.
32	V <sub>DD</sub>	Power	Power supply for Core and input Buffer blocks, 3.3V.

**Table 1: Pin Descriptions<sup>1</sup> (Continued)**

Number	Name	Type		Description
33	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to 0.5V <sub>DD</sub> .
34	CLK1	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
35	V <sub>DD</sub>	Power		Power supply for Core and input Buffer blocks, 3.3V
36	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
37	VDDOC	Power		Output supply pin for REFOUT output.
38	OE_SE	Input	Pulldown	REFOUT output enable.
39	VDD	Power		Power supply for Core and input Buffer blocks, 3.3V.
40	GND	Power		Ground.
ePad	GND_EP	Power		Connect ePad to ground to ensure proper heat dissipation.

NOTE 1. *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2: Pin Characteristics**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	OE_SE, SMODEx[1:0], REF_SEL[1:0]			2		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				50		kΩ
R <sub>PULLUP</sub>	Input Pullup/down Resistor	nCLK0			40/40		kΩ
		nCLK1			40/40		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance	REFOUT	VDDOC = 3.465V		5.3		pF
		REFOUT	VDDOC = 2.625V		6.3		pF
R <sub>OUT</sub>	Output Impedance	REFOUT	VDDOC = 3.3V		50		Ω
		REFOUT	VDDOC = 2.5V		60		Ω

## Function Tables

Table 3: REF\_SELx Function Table

Control Input	Selected Input Reference Clock
REF_SEL[1:0]	
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 4: OE\_SE Function Table<sup>1</sup>

OE_SE	REFOUT
0 (default)	High-Impedance
1	Enabled

NOTE 1. Synchronous output enable to avoid clock glitch.

Table 5: Input/Output Operation Table, OE\_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0 (default)	Don't care	Don't Care	High Impedance
1	10 or 11	Don't Care	Fanout crystal oscillator
1	00 (default)	CLK0 and nCLK0 are both open circuit	Logic Low
		CLK0 and nCLK0 are tied to ground	Logic Low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic Low
		CLK1 and nCLK1 are tied to ground	Logic Low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

Table 6: Input/Output Operation Table, CLKoutA\_EN

Input Status			Output State
CLKoutA_EN	REF_SEL[1:0]	CLKx and nCLKx	QA[3:0], nQA[3:0]
1	Don't care	Don't Care	High Impedance
0	10 or 11	Don't Care	Fanout crystal oscillator
0	00 (default)	CLK0 and nCLK0 are both open circuit	QA[3:0] = Low nQA[3:0] = High
		CLK0 and nCLK0 are tied to ground	QA[3:0] = Low nQA[3:0] = High
		CLK0 is high, nCLK0 is low	QA[3:0] = High nQA[3:0] = Low
		CLK0 is low, nCLK0 is high	QA[3:0] = Low nQA[3:0] = High
0	01	CLK1 and nCLK1 are both open circuit	QA[3:0] = Low nQA[3:0] = High
		CLK1 and nCLK1 are tied to ground	QA[3:0] = Low nQA[3:0] = High
		CLK1 is high, nCLK1 is low	QA[3:0] = High nQA[3:0] = Low
		CLK1 is low, nCLK1 is high	QA[3:0] = Low nQA[3:0] = High

**Table 7: Input/Output Operation Table, CLKoutB\_EN**

Input Status			Output State
CLKoutB_EN	REF_SEL[1:0]	CLKx and nCLKx	QB[3:0], nQB[3:0]
1	Don't care	Don't Care	High Impedance
0	10 or 11	Don't Care	Fanout crystal oscillator
0	00 (default)	CLK0 and nCLK0 are both open circuit	QB[3:0] = Low nQB[3:0] = High
		CLK0 and nCLK0 are tied to ground	QB[3:0] = Low nQB[3:0] = High
		CLK0 is high, nCLK0 is low	QB[3:0] = High nQB[3:0] = Low
		CLK0 is low, nCLK0 is high	QB[3:0] = Low nQB[3:0] = High
0	01	CLK1 and nCLK1 are both open circuit	QB[3:0] = Low nQB[3:0] = High
		CLK1 and nCLK1 are tied to ground	QB[3:0] = Low nQB[3:0] = High
		CLK1 is high, nCLK1 is low	QB[3:0] = High nQB[3:0] = Low
		CLK1 is low, nCLK1 is high	QB[3:0] = Low nQB[3:0] = High

**Table 8: Output Level Selection Table**

CLKoutA_EN	Output Type
0	HCSL
1	HiZ

CLKoutB_EN	Output Type
0	HCSL
1	HiZ

## Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
$V_{DD}, V_{DDOX}^1$	4.6V
$V_{IN}$	-0.3V to $V_{DDOX}^1 + 0.3V$
$T_J$ : Junction Temperature	150°C
$T_{STG}$ : Storage Temperature	-65°C to 150°C

NOTE 1.  $V_{DDOX}$  denotes  $V_{DDOA}, V_{DDOB}$  and  $V_{DDOC}$ .

## ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

## Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
$T_A$	Ambient air temperature	-40		85	°C
$T_J$	Junction temperature			125	°C
$V_{DD}$	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
$V_{DDOX}^1$	Power supply for Bank QA or QB or REFOUT	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	

NOTE 1.  $V_{DDOX}$  denotes  $V_{DDOA}, V_{DDOB}$  and  $V_{DDOC}$ .

## Electrical Characteristics

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T<sub>A</sub> ≤ 85 °C, CLK<sub>in</sub> driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T<sub>A</sub> = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>Current Consumption<sup>(2)</sup></b>						
I <sub>DD_CORE</sub>	Core Supply Current, All Outputs Disabled	CLK_X selected		11.5		mA
		XTAL selected		21.5		mA
I <sub>DD_HCSL</sub>	Additive Core Supply Current, Per HCSL Bank Enabled			14.8		mA
I <sub>DD_CMOS</sub>	Additive Core Supply Current, LVCMOS Output Enabled			3.4		mA
I <sub>DDO_HCSL</sub>	Additive Output Supply Current, Per HCSL Bank Enabled	Includes Output Bank Bias and Load Currents, R <sub>T</sub> = 50 Ω on all outputs in bank		95		mA
I <sub>DDO_CMOS</sub>	Additive Output Supply Current, LVCMOS Output Enabled	200 MHz, C <sub>L</sub> = 5 pF		1.6		mA
<b>Power Supply Ripple Rejection (PSRR)</b>						
PSRR <sub>HCSL</sub>	Ripple-Induced Phase Spur Level <sup>(3)</sup> Differential HCSL Output	100 kHz, 100 mVpp Ripple Injected on VDDO, VDDO = 3.3 V @156.25 MHz		-76		dBc
<b>CMOS Control Inputs (REF_SEL[1:0], CLKoutA_EN, CLKoutB_EN, OE_SE)</b>						
V <sub>IH</sub>	High-Level Input Voltage		1.65		VDD	V
V <sub>IL</sub>	Low-Level Input Voltage		GND		1.5	V
I <sub>IH</sub>	High-Level Input Current	V <sub>IH</sub> = VDD, Internal pull-down resistor			67	μA
I <sub>IL</sub>	Low-Level Input Current	V <sub>IL</sub> = 0 V, Internal pull-down resistor	-5	0.2		μA
<b>Universal Clock Inputs (CLK0/nCLK0, CLK1/nCLK1)</b>						
f <sub>CLKin</sub>	Input Frequency Range <sup>(4)</sup>	Functional up to 400MHz Output frequency range and timing specified per output type (refer to HCSL, LVCMOS output specifications)	DC		400	MHz
V <sub>IHD</sub>	Differential Input High Voltage	CLK <sub>in</sub> driven differentially			VDD	V
V <sub>ILD</sub>	Differential Input Low Voltage		GND			V
V <sub>ID</sub>	Differential Input Voltage Swing <sup>(5)</sup>		0.15		1.3	V
V <sub>CMD</sub>	Differential Input Common Mode Voltage	V <sub>ID</sub> = 150 mV	0.25		VDD - 1.2	V
		V <sub>ID</sub> = 350 mV	0.25		VDD - 1.1	
		V <sub>ID</sub> = 800 mV	0.25		VDD - 0.9	
V <sub>IH</sub>	Single-Ended Input High Voltage	CLK_X driven single-ended (AC or DC coupled), nCLK_X AC coupled to GND or externally biased within V <sub>CM</sub> range			VDD	V
V <sub>IL</sub>	Single-Ended Input Low Voltage		GND			V
V <sub>I_SE</sub>	Single-Ended Input Voltage Swing		0.3		2	V <sub>pp</sub>
V <sub>CM</sub>	Single-Ended Input Common Mode Voltage		0.25		VDD - 1.2	V
ISO <sub>MUX</sub>	Mux Isolation, CLK0 to CLK1		f <sub>OFFSET</sub> > 50 kHz, P <sub>CLK_X</sub> = 0 dBm	f <sub>CLK0</sub> = 100 MHz		-112.5
<b>Crystal Interface (XTAL_I, XTAL_O)</b>						
F <sub>CLK</sub>	External Clock Frequency Range <sup>(4)</sup>	XTAL_I driven single-ended, XTAL_O floating			250	MHz
F <sub>XTAL</sub>	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) <sup>(6)</sup>	10		48	MHz
C <sub>IN</sub>	XTAL Input Capacitance			4		pF

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(2) See *Power Considerations* for more information on current consumption and power dissipation calculations.

(3) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the VDDO supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [ (2 \* 10<sup>(PSRR / 20)</sup>) / (π \* f<sub>CLK</sub>) ] \* 1E12

## Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, TA = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>Universal Clock Inputs (CLK0/nCLK0, CLK1/nCLK1)</b>						
f <sub>CLKin</sub>	Input Frequency Range <sup>(4)</sup>	Functional up to 400MHz Output frequency range and timing specified per output type (refer to HCSL, LVCMOS output specifications)	DC		400	MHz
V <sub>IHD</sub>	Differential Input High Voltage	CLKin driven differentially			VDD	V
V <sub>ILD</sub>	Differential Input Low Voltage				GND	V
V <sub>ID</sub>	Differential Input Voltage Swing		0.15		1.3	V
V <sub>CMD</sub>	Differential Input Common Mode Voltage		V <sub>ID</sub> = 150 mV V <sub>ID</sub> = 350 mV V <sub>ID</sub> = 800 mV	0.25	VDD - 1.2	
V <sub>IH</sub>	Single-Ended Input High Voltage	CLK_X driven single-ended (AC or DC coupled), nCLK_X AC coupled to GND or externally biased within V <sub>CM</sub> range			VDD	V
V <sub>IL</sub>	Single-Ended Input Low Voltage				GND	V
V <sub>I_SE</sub>	Single-Ended Input Voltage Swing <sup>(6)(7)</sup>		0.3		2	V <sub>pp</sub>
V <sub>CM</sub>	Single-Ended Input Common Mode Voltage		0.25		VDD - 1.2	V
ISO <sub>MUX</sub>	Mux Isolation, CLK0 to CLK1	f <sub>OFFSET</sub> > 50 kHz, P <sub>CLK_X</sub> = 0 dBm	f <sub>CLK0</sub> = 100 MHz		-112.5	dBc
<b>Crystal Interface (XTAL_I, XTAL_O)</b>						
F <sub>CLK</sub>	External Clock Frequency Range <sup>(4)</sup>	XTAL_I driven single-ended, XTAL_O floating			250	MHz
F <sub>XTAL</sub>	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) <sup>(8)</sup>		10	48	MHz
C <sub>IN</sub>	XTAL Input Capacitance				4	pF

(4) Specification is ensured by characterization and is not tested in production.

(5) See V<sub>ID</sub> = Differential input Voltage Swing, V<sub>OD</sub> = Differential output Voltage Swing.

(6) Parameter is specified by design, not tested in production.

(7) For clock input frequency ≥ 100 MHz, CLK\_X can be driven with single-ended (LVCMOS) input swing up to 3.3 V<sub>pp</sub>. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 V<sub>pp</sub> max to prevent input saturation.

(8) The ESR requirements stated must be met to ensure that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal.

## Electrical Characteristics(Output)

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T<sub>A</sub> ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T<sub>A</sub> = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.<sup>(1)</sup>

Parameter		Test Conditions		Min	Typ	Max	Unit	
<b>HCSL Outputs</b>								
f <sub>CLKout</sub>	Output Frequency Range <sup>(9)</sup>	R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		DC		400	MHz	
Jitter <sub>ADD</sub>	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz <sup>(10)</sup>	VDDO = 3.3 V, R <sub>T</sub> = 50 Ω to GND	CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		70		fs	
Noise Floor	Noise Floor; f <sub>OFFSET</sub> ≥ 10 MHz <sup>(13)</sup> (14)	VDDO = 3.3 V, R <sub>T</sub> = 50 Ω to GND	CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		-160		dBc/Hz	
DUTY	Duty Cycle <sup>(4)</sup>	50% input clock duty cycle		45%		55%		
V <sub>OH</sub>	Output High Voltage	T <sub>A</sub> = 25 °C, DC Measurement, R <sub>T</sub> = 50 Ω to GND		520	800	920	mV	
V <sub>OL</sub>	Output Low Voltage			-150	0.5	150	mV	
V <sub>CROSS</sub>	Absolute Crossing Voltage <sup>(4)</sup> (15)	R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		160	350	460	mV	
ΔV <sub>CROSS</sub>	Total Variation of V <sub>CROSS</sub>					140	mV	
t <sub>F</sub>	Output Fall Time 80% to 20% <sup>(6)</sup> (15)				300	500	ps	
<b>LVC MOS Output (REFOUT)</b>								
f <sub>CLKout</sub>	Output Frequency Range <sup>(4)</sup>	C <sub>L</sub> ≤ 5 pF		DC		250	MHz	
Jitter <sub>ADD</sub>	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz <sup>(10)</sup>	VDDO = 3.3 V, C <sub>L</sub> ≤ 5 pF	156.25 MHz, Input Slew rate ≥ 3 V/ns		61		fs	
Noise Floor	Noise Floor f <sub>OFFSET</sub> ≥ 10 MHz <sup>(13)</sup> (14)	VDDO = 3.3 V, C <sub>L</sub> ≤ 5 pF	156.25 MHz, Input Slew rate ≥ 3 V/ns		-160		dBc/Hz	
DUTY	Duty Cycle <sup>(4)</sup>	50% input clock duty cycle		45%		55%		
V <sub>OH</sub>	Output High Voltage	1 mA load			VDDO-0.1		V	
V <sub>OL</sub>	Output Low Voltage			0.1				V
I <sub>OH</sub>	Output High Current (Source)	V <sub>O</sub> = VDDO / 2		VDDO = 3.3 V	28		mA	
				VDDO = 2.5 V	20			
I <sub>OL</sub>	Output Low Current (Sink)			VDDO = 3.3 V	28		mA	
				VDDO = 2.5 V	20			
t <sub>R</sub>	Output Rise Time 20% to 80% <sup>(6)</sup> (15)	250 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R <sub>L</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF			225	400	ps	
t <sub>F</sub>	Output Fall Time 80% to 20% <sup>(6)</sup> (15)				225	400	ps	
t <sub>EN</sub>	Output Enable Time <sup>(16)</sup>	C <sub>L</sub> ≤ 5 pF				3	cycles	
t <sub>DIS</sub>	Output Disable Time <sup>(16)</sup>					3	cycles	
<b>Propagation Delay and Output Skew</b>								
t <sub>PD_HCSL</sub>	Propagation Delay CLKin-to- HCSL <sup>(6)</sup> (15)	R <sub>T</sub> = 50 Ω to GND, C <sub>L</sub> ≤ 5 pF		295	590	885	ps	
t <sub>PD_CMOS</sub>	Propagation Delay CLKin-to- LVC MOS <sup>(6)</sup> (15)	C <sub>L</sub> ≤ 5 pF		VDDO = 3.3 V	900	1475	2300	ps
				VDDO = 2.5 V	1000	1550	2700	
t <sub>SK(O)</sub>	Output Skew LVPECL/LVDS/HCSL <sup>(4)</sup> (15)(17)	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.			30	50	ps	
t <sub>SK(PP)</sub>	Part-to-Part Output Skew LVPECL/LVDS/HCSL <sup>(6)</sup> (15)(17)				80	120	ps	

(9) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

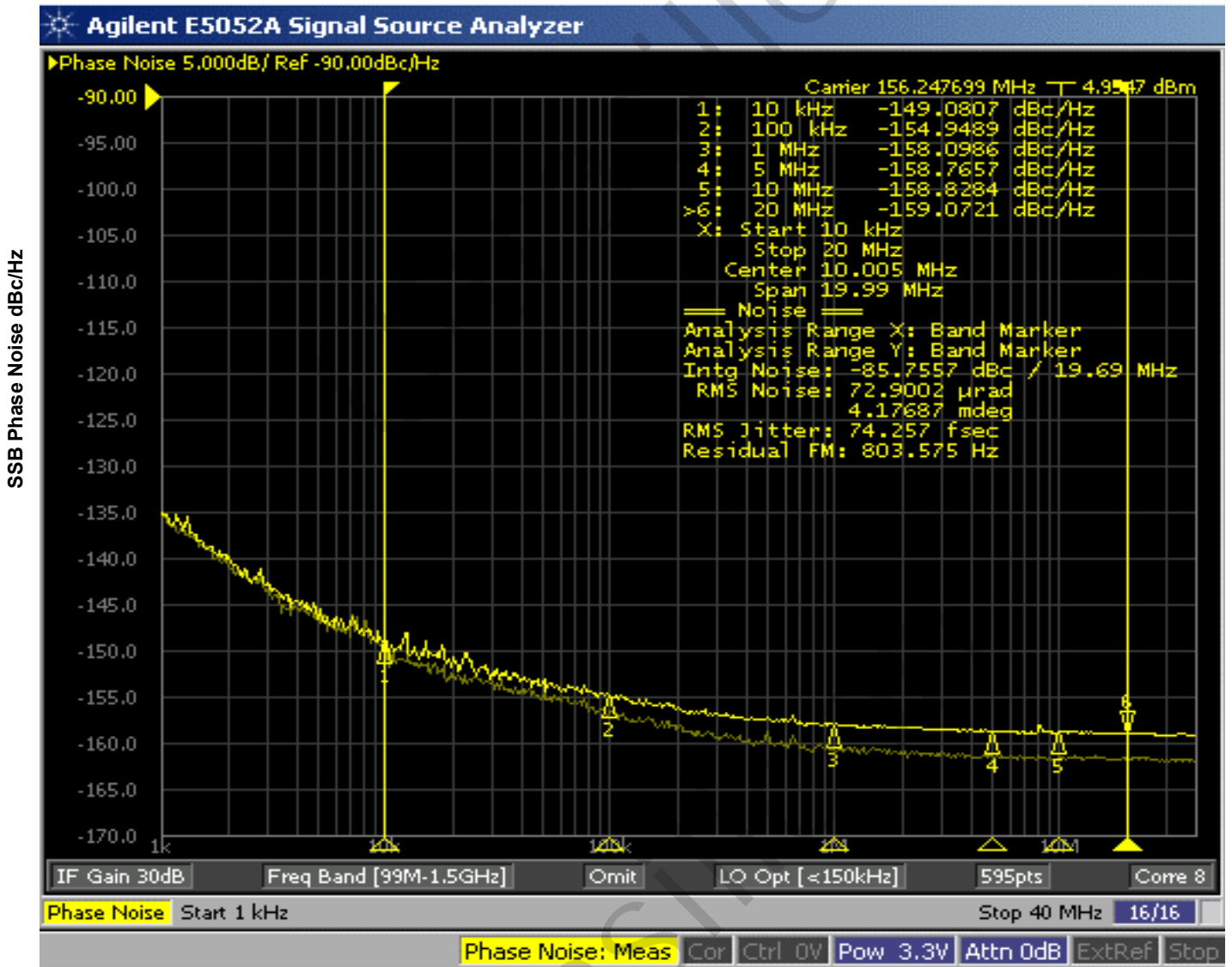
(10) Output Enable Time is the number of input clock cycles it takes for the output to be enabled after OE\_SE is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after OE\_SE is pulled low. The OE\_SE signal should have an edge transition much faster than that of the input clock period for accurate measurement.

(11) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



Offset from Carrier Frequency (Hz)

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using an EPSON Clock Driver SG3225VEN as an input source and Agilent E5052A phase noise analyzer.

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, 1kΩ resistors can be tied from CLK to ground and nCLK to V<sub>DD</sub>.

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_I and XTAL\_O can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_I to ground.

##### LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Input Interface

The US5D338 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2*. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

#### Power Up Ramp Sequence

This device has multiple supply pins dedicated for different blocks. Output power supplies V<sub>DDOx</sub> (V<sub>DDOA</sub>, V<sub>DDOB</sub>, V<sub>DDOC</sub>) must ramp up after, or concurrently with core power supply V<sub>DD</sub>. All power supplies must ramp up in a linear fashion and monotonically. Both V<sub>DDOA</sub> and V<sub>DDOB</sub> power supplies must be powered-up even when only one bank of outputs is in use.

#### Outputs:

##### LVC MOS Output (REFOUT)

If LVC MOS output is not used, then disable the output and it can be left floating.

##### HCSL Outputs

Any unused output pairs can be left floating. We recommend that there is no trace attached.

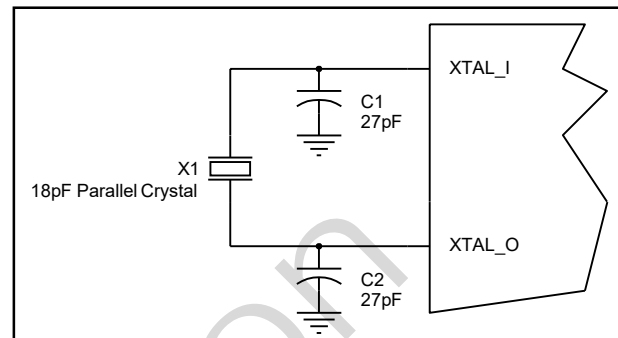


Figure 1: Crystal Input Interface

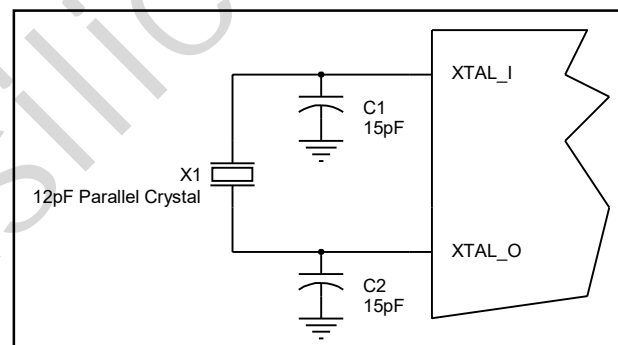


Figure 2: Crystal Input Interface

## Overdriving the XTAL Interface

The XTAL\_I input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_O pin can be left floating. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 4 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_I input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

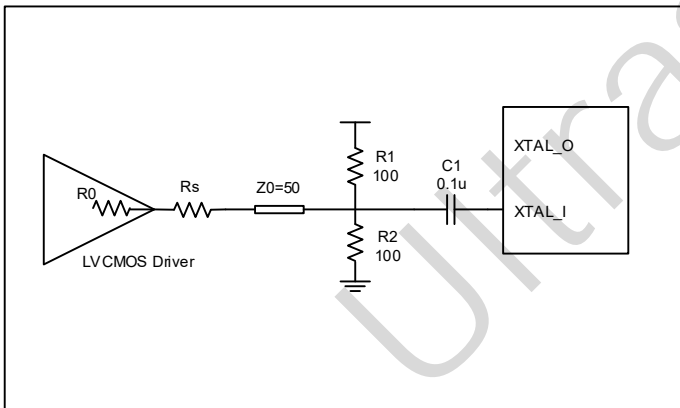


Figure 3: General Diagram for LVCMOS Driver to XTAL Input Interface

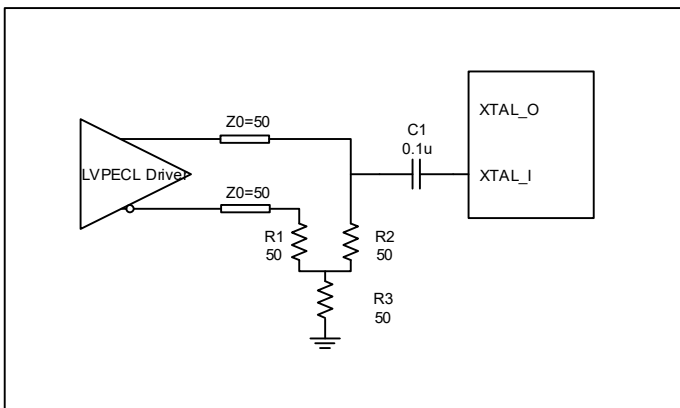


Figure 4: General Diagram for LVPECL Driver to XTAL Input Interface

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{DD} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3V$ . Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

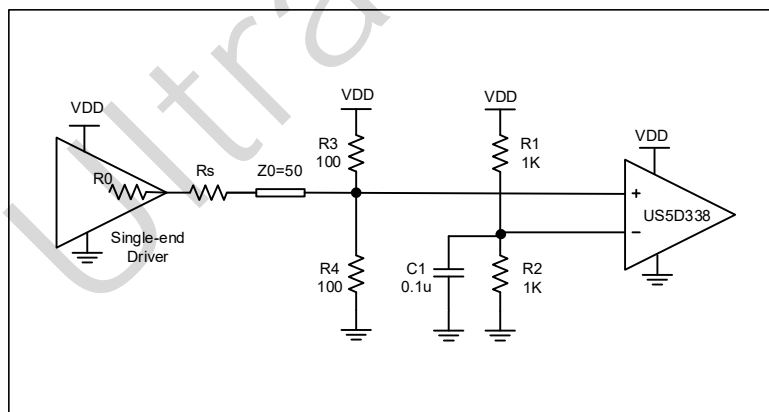


Figure 5: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

### 3.3V Differential Clock Input Interface

The CLK/nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figure 6 to Figure 9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

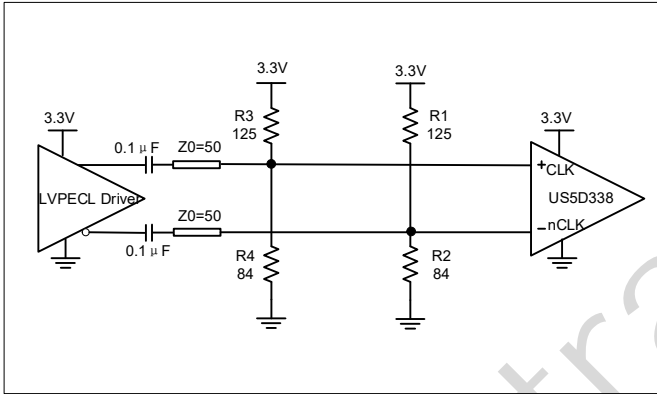


Figure 6: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

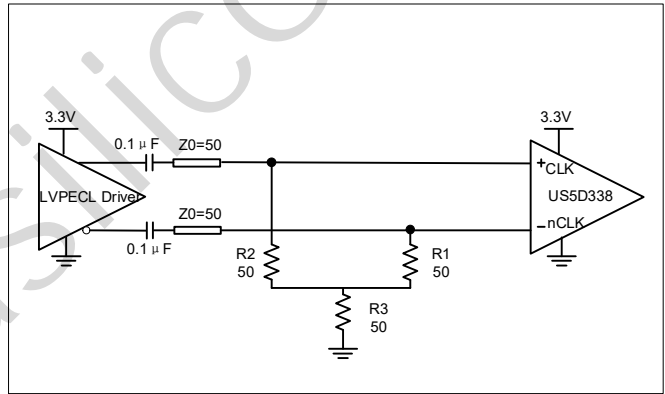


Figure 8: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

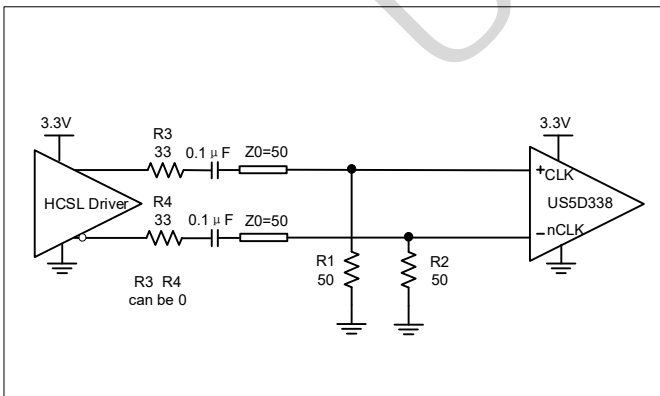


Figure 7: CLK/nCLK Input Driven by a 3.3V HCSL Driver

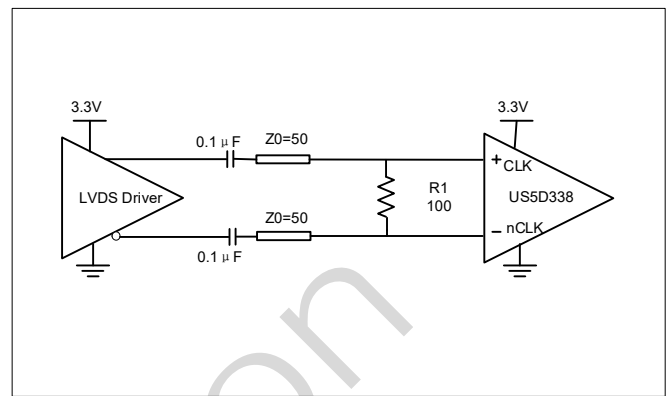


Figure 9: CLK/nCLK Input Driven by a 3.3V LVDS Driver

## 2.5V Differential Clock Input Interface

The CLK/nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figure 10 to Figure 13 show interface examples for the CLK/nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

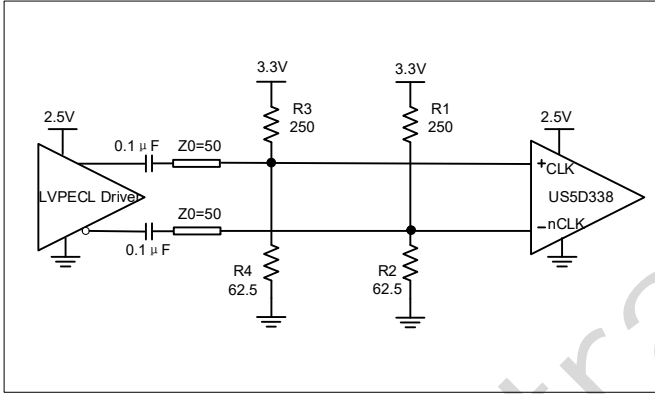


Figure 10: CLK/nCLK Input Driven by a 2.5V LVPECL Driver

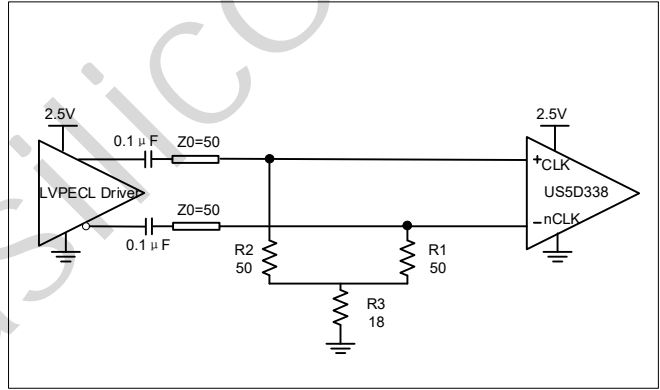


Figure 11: CLK/nCLK Input Driven by a 2.5V LVPECL Driver

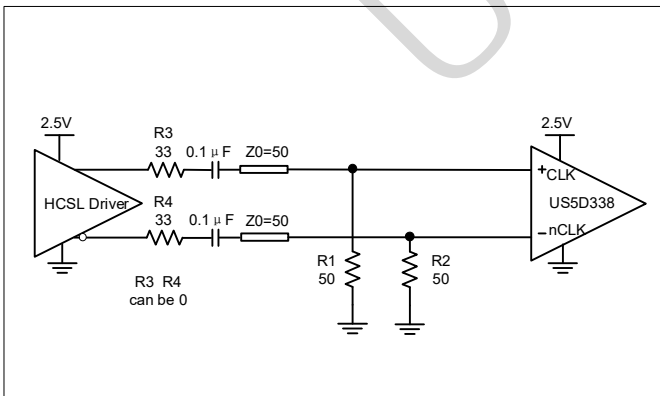


Figure 12: CLK/nCLK Input Driven by a 2.5V HCSL Driver

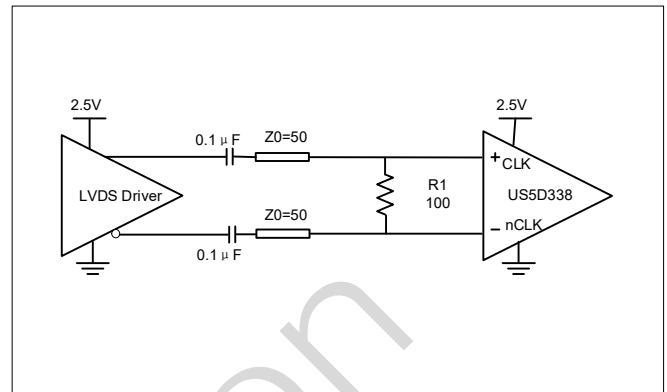


Figure 13: CLK/nCLK Input Driven by a 2.5V LVDS Driver

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in Figure 14 can be used.

Figure 15, which can also be used, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ .

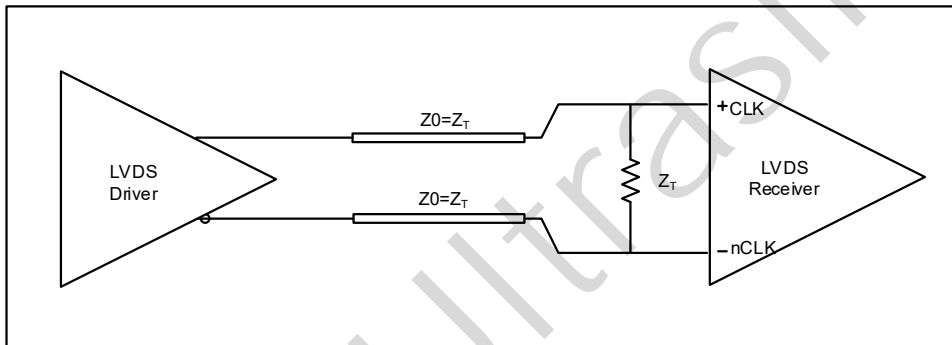


Figure 14: Standard LVDS Termination

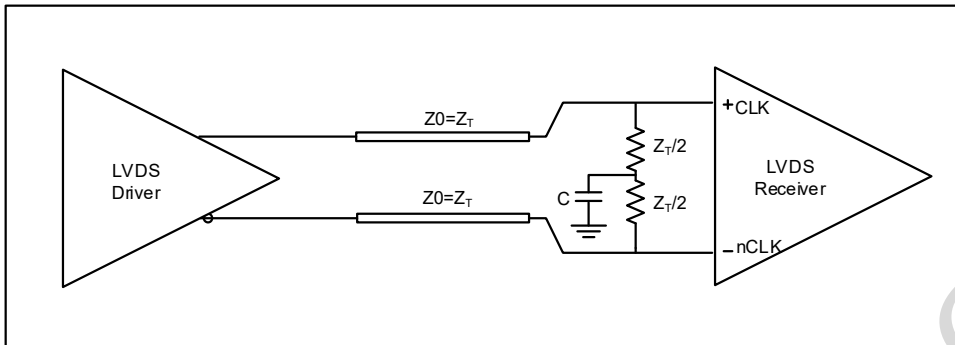
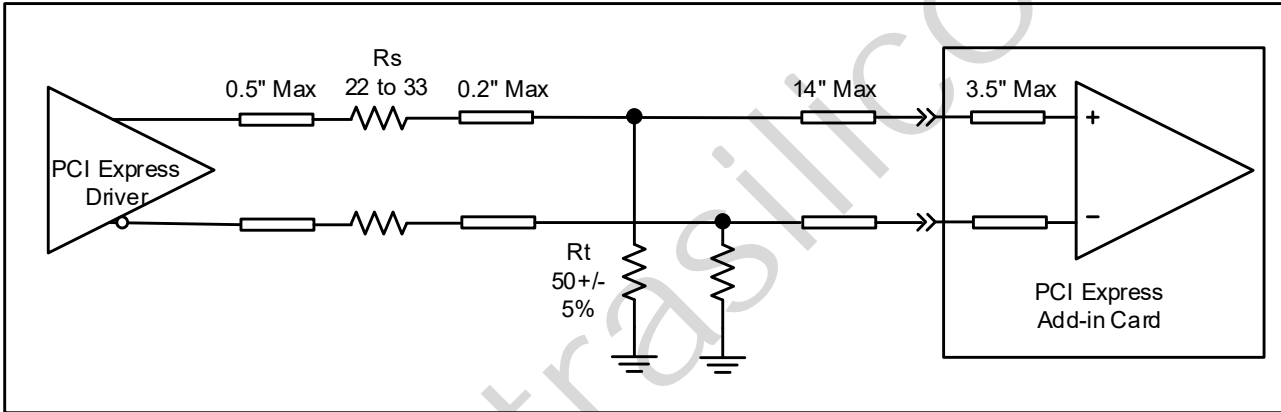


Figure 15: Optional LVDS Termination

### Recommended Termination

Figure 16 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

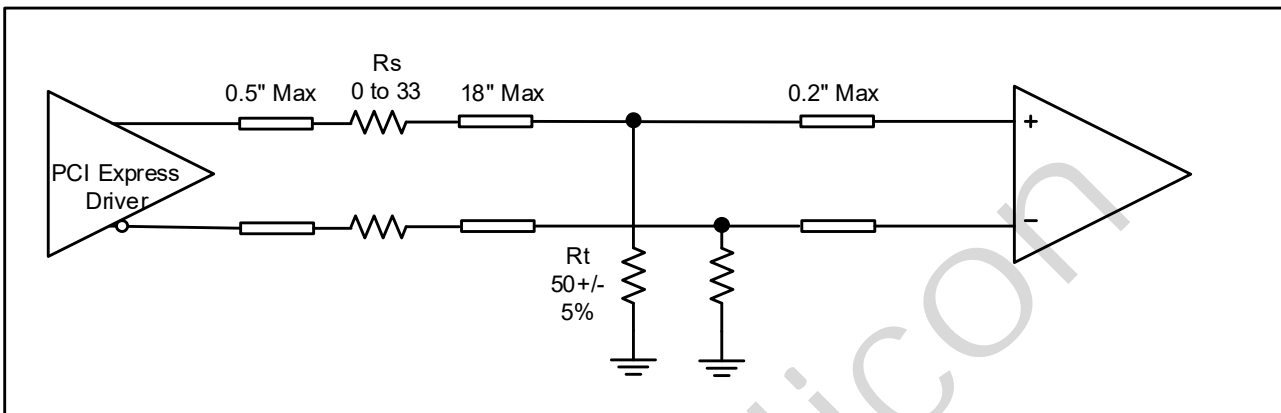
types. All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 16: Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

Figure 17 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor ( $R_s$ ) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 17: Recommended Termination (where a point-to-point connection can be used)**

### WQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 23*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only.

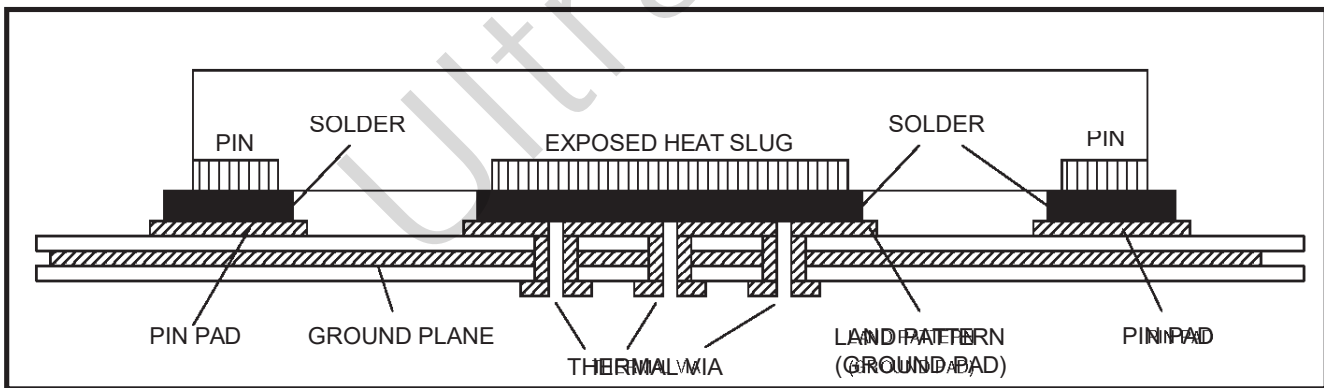
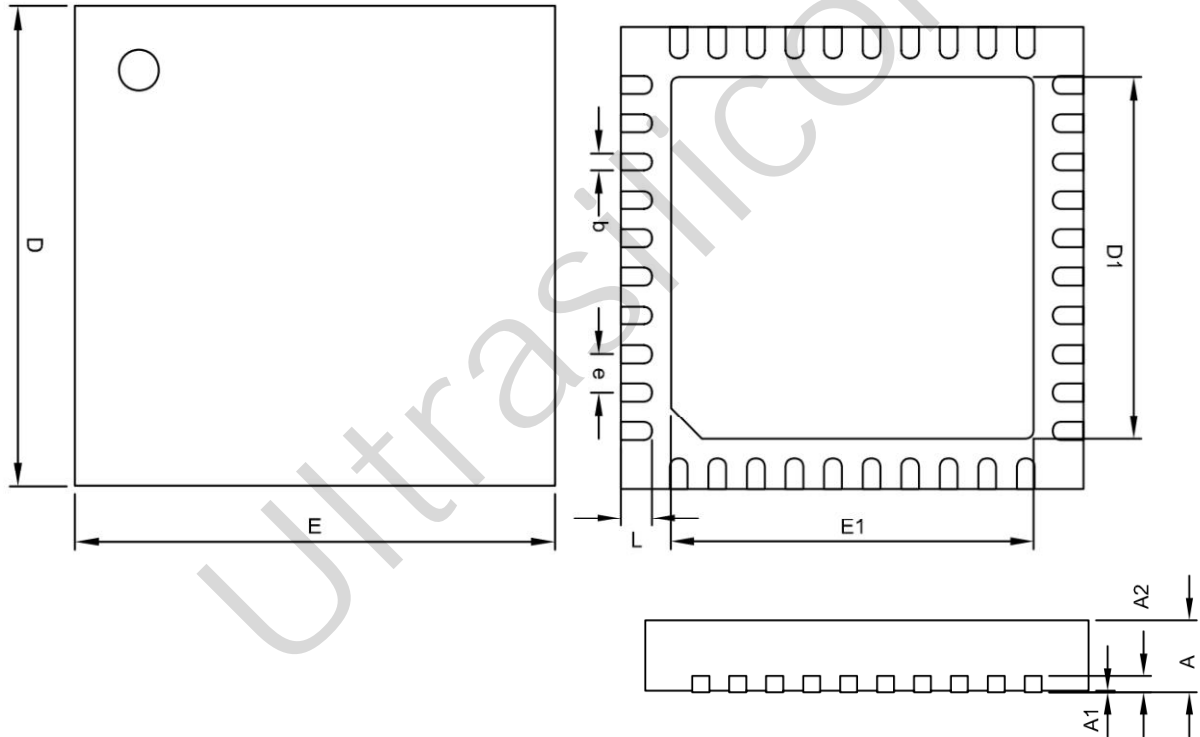


Figure 23: P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

### PACKAGE DIMENSIONS



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.55	4.65	4.75	0.1791	0.1831	0.1870
E1	4.55	4.65	4.75	0.1791	0.1831	0.1870
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

### Reflow profile

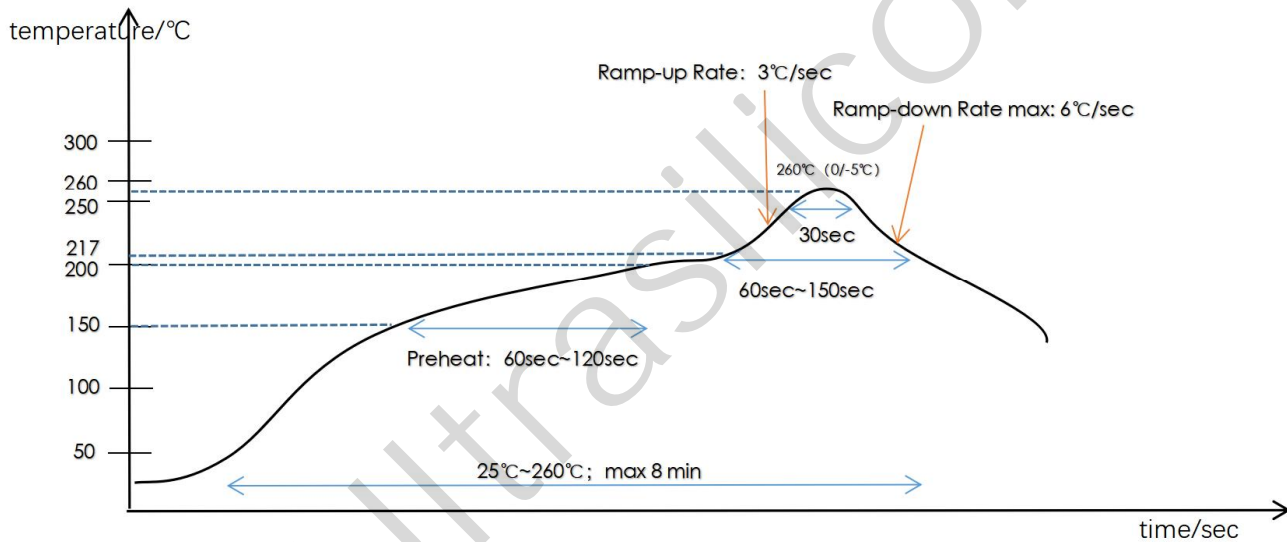


Figure24: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

## Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0

Ultrasilicon