Description

The US5D104D is a low skew, high performance 1-to-4 clock fanout buffer. Utilizing Low Voltage Differential Signaling (LVDS) the US5D104D provides a low power, low noise, solution for distributing clock signals. The US5D104D accepts differential input level and translates it to LVDS output levels. Guaranteed output and part-to-part skew characteristics make the US5D104D ideal for those applications demanding well defined performance and repeatability.

The US5D104D clock buffer distributes one clock input to 4 pairs of differential LVDS clock outputs with minimum skew for clock distribution. The inputs can either be LVDS,LVPECL, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal.

Features

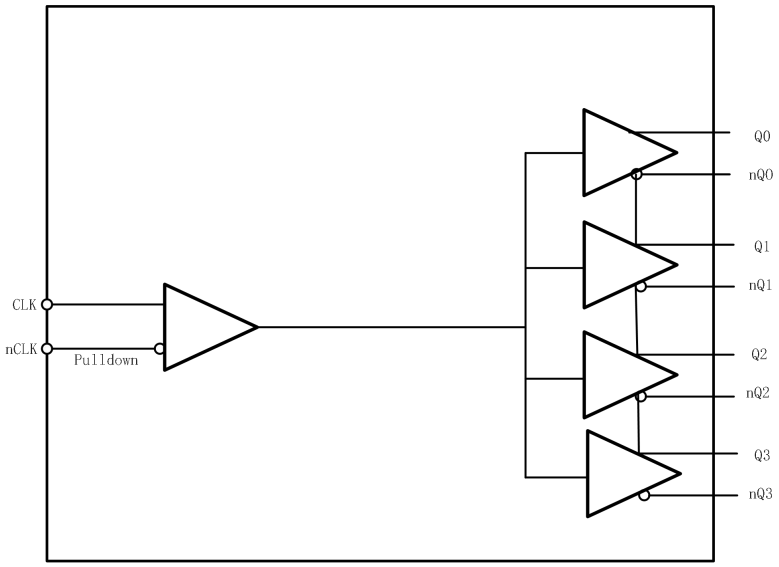
- 1:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS and LVCMOS
- Four LVDS outputs
- Maximum Output

  Frequence LVDS - 2-GHz
- Propagation Delay: 0.5 ns(typical)
- Output skew: 50 ps (Maximum)
- Part-to-part skew: 300ps (Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz: 53 fs RMS (12kHz - 20MHz)
- 3.3V or 2.5V operating supply
- Industrial Temperature Range:-40°C to 85°C
- Available in TSSOP-16 package

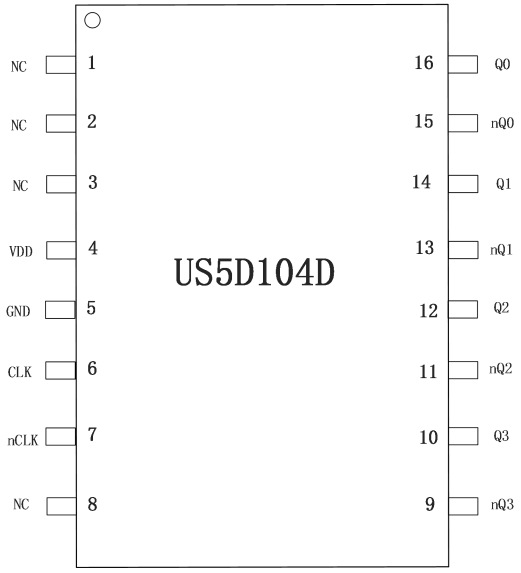
Applications

- Clock Distribution
- Wireless Base Stations
- Network Routers

Block Diagram



Pin Assignment for TSSOP-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
6	CLK	Input	differential input or single-ended input.
7	nCLK	Input	differential input.
1	NC	---	No connect
2	NC	---	No connect
3	NC	---	No connect
8	NC	---	No connect
5	GND	Power	Ground
4	VDD	Power	Power supply for Core.
16	Q0	Output	Differential LVDS clock output pair.
15	nQ0	Output	Differential LVDS clock output pair.
14	Q1	Output	Differential LVDS clock output pair.
13	nQ1	Output	Differential LVDS clock output pair.
12	Q2	Output	Differential LVDS clock output pair.
11	nQ2	Output	Differential LVDS clock output pair.
10	Q3	Output	Differential LVDS clock output pair.
9	nQ3	Output	Differential LVDS clock output pair.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1500	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

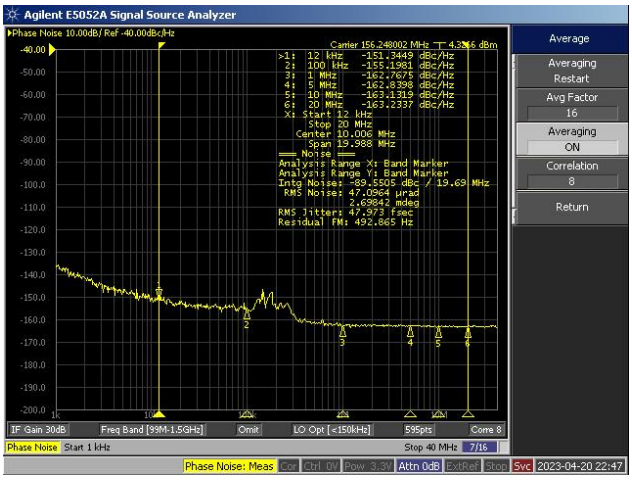
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	V

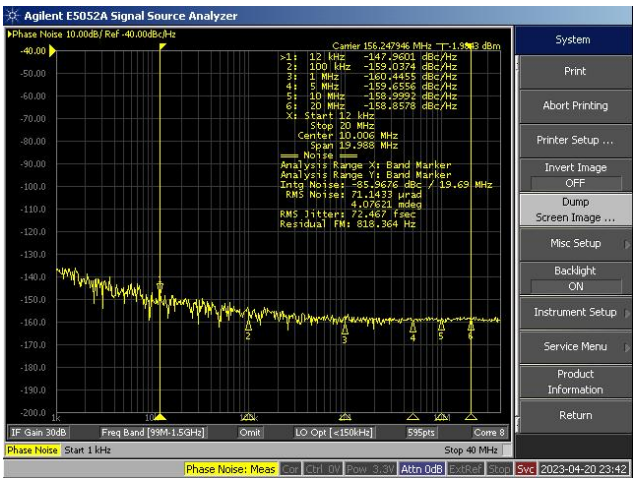
Electrical Characteristics

VDD = 3.135 V to 3.465 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
FIN	Input Frequency	VDD=3.3V	0.1		2000	MHz
VOD	Differential output voltage magnitude	T_A = 25 °C, DC Measurement, R_L = 100 Ω differential	250	400	450	mV
ΔVOD	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	T_A = 25 °C, DC Measurement, R_L = 100 Ω differential	1.125		1.375	V
Δ $V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
Icc	Supply current	Enabled, RL = 100 Ω		74		mA
I_{IH}	High-level input current (enables)	VIH = 2 V			20	uA
I_{IL}	Low-level input current (enables)	VIL = 0.8 V			10	uA
C_{IN}	Input capacitance			3		pF
t_r	Differential output signal rise time	RL = 100 Ω		100	300	ps
t_f	Differential output signal fall time	RL = 100 Ω		100	300	ps
$t_{sk(o)}$	Channel-to-channel output skew	RL = 100 Ω		20	50	ps
$t_{sk(pp)}$	Part-to-part skew				300	ps
t_{PD}	Propagation delay	VIN, DIFF, PP = 0.3 V		0.5	1.5	ns
$Jitter_{ADD}$	Additive jitter	156.25MHz, Integration Bandwidth 12KHz to 20MHz, VDD=3.3V		53	100	fs

Phase Noise Plot





Low jitter SPXO(156.25MHz)(48fs) Output Phase Noise(72fs)

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

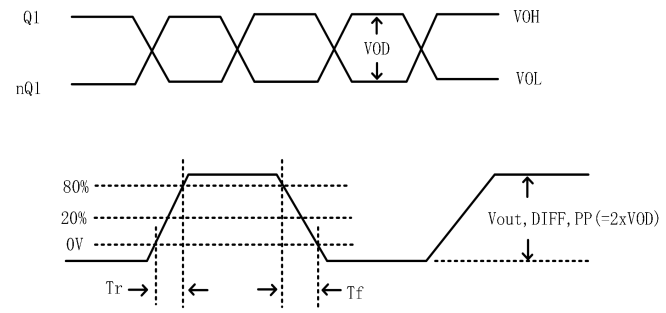
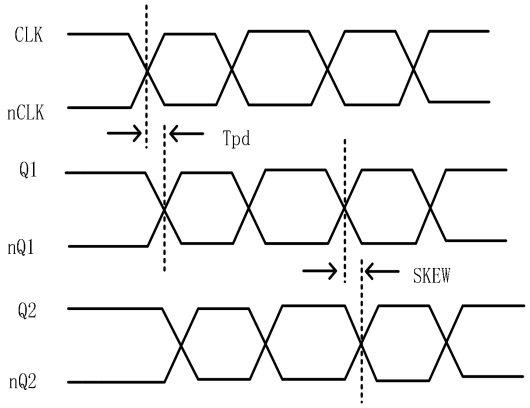


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 2.output and skew

Applications Information

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

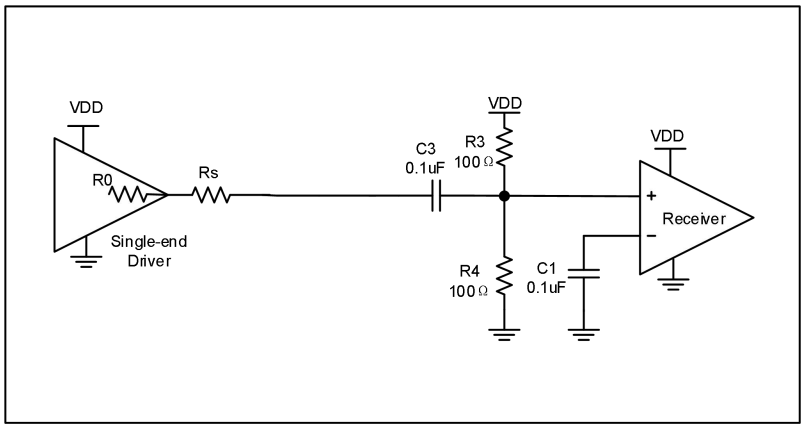
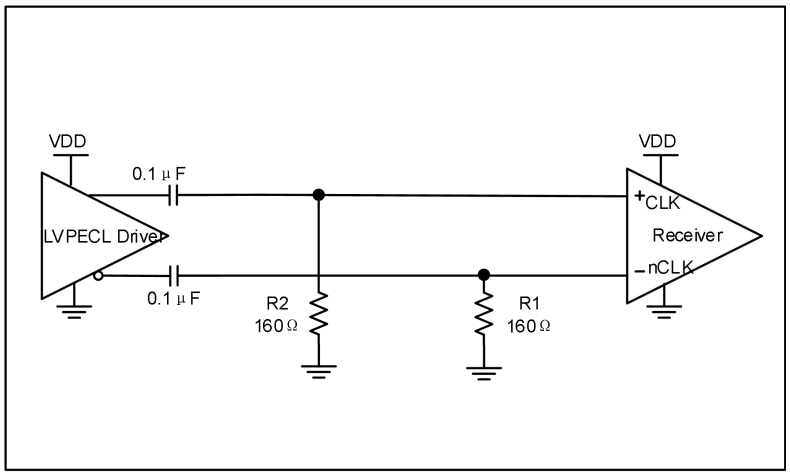
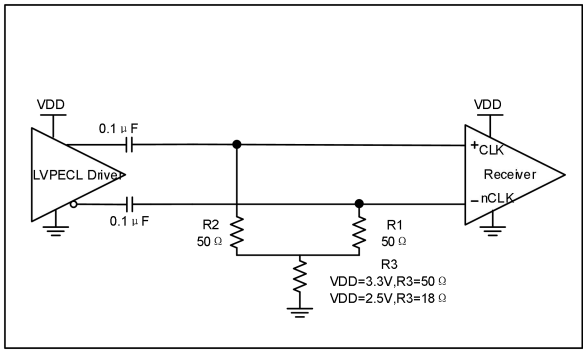


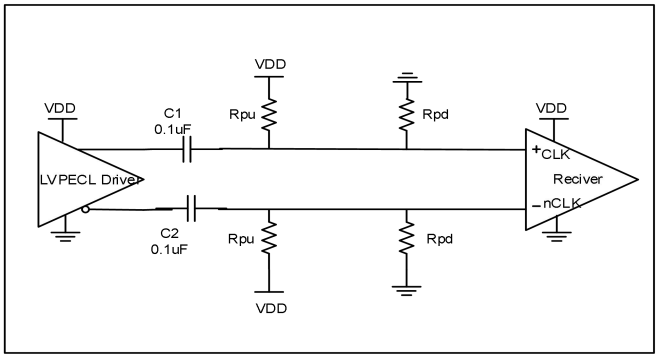
Figure3.Single-termination method of differential input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure4 to Figure7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

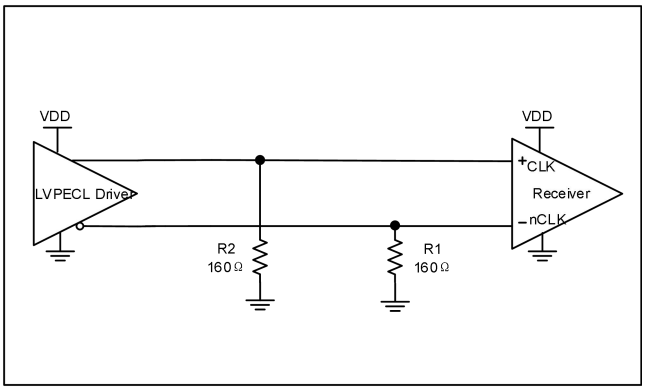


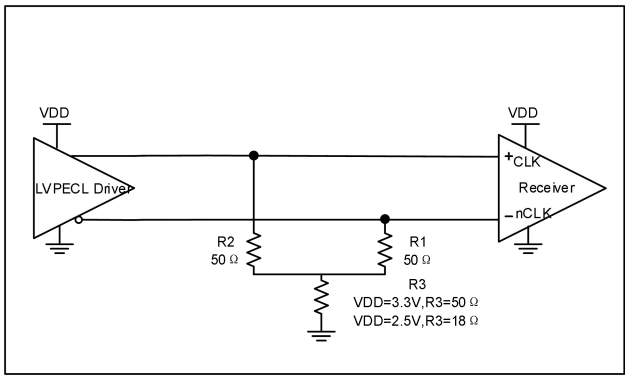


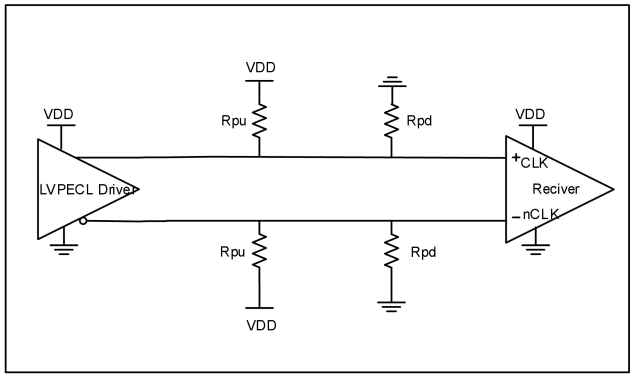


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure4.LVPECL Driver(AC)

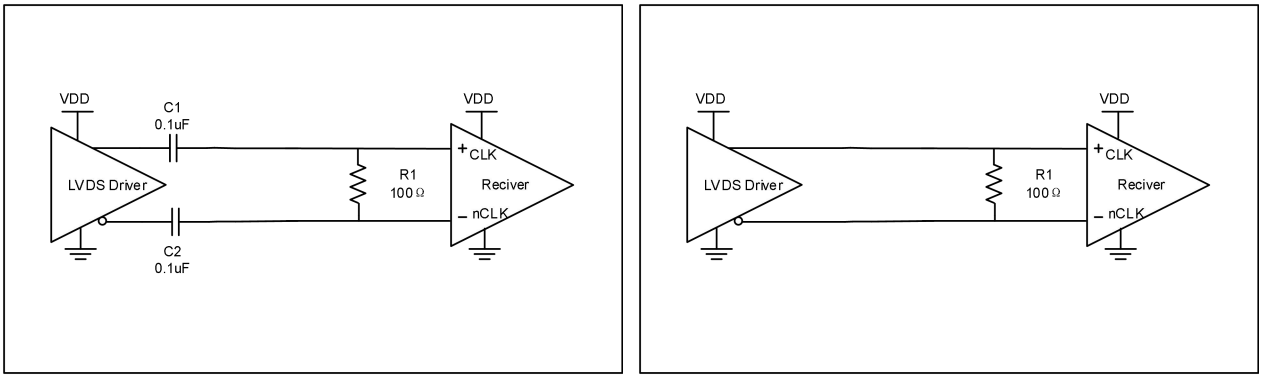






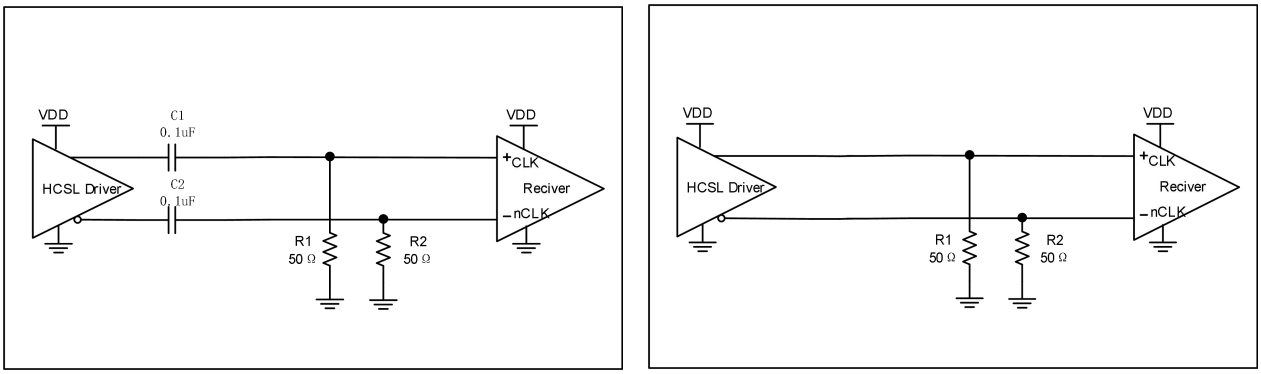
VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

Figure6.LVDS Driver



a)AC coupling **b)DC coupling**

Figure7.HCSL Driver

Output connection circuit

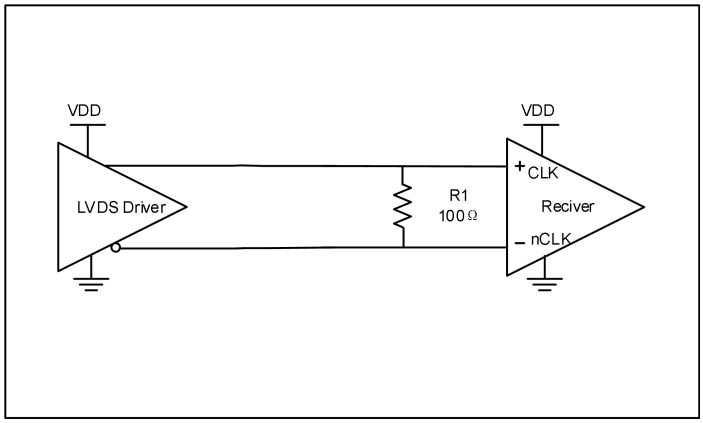
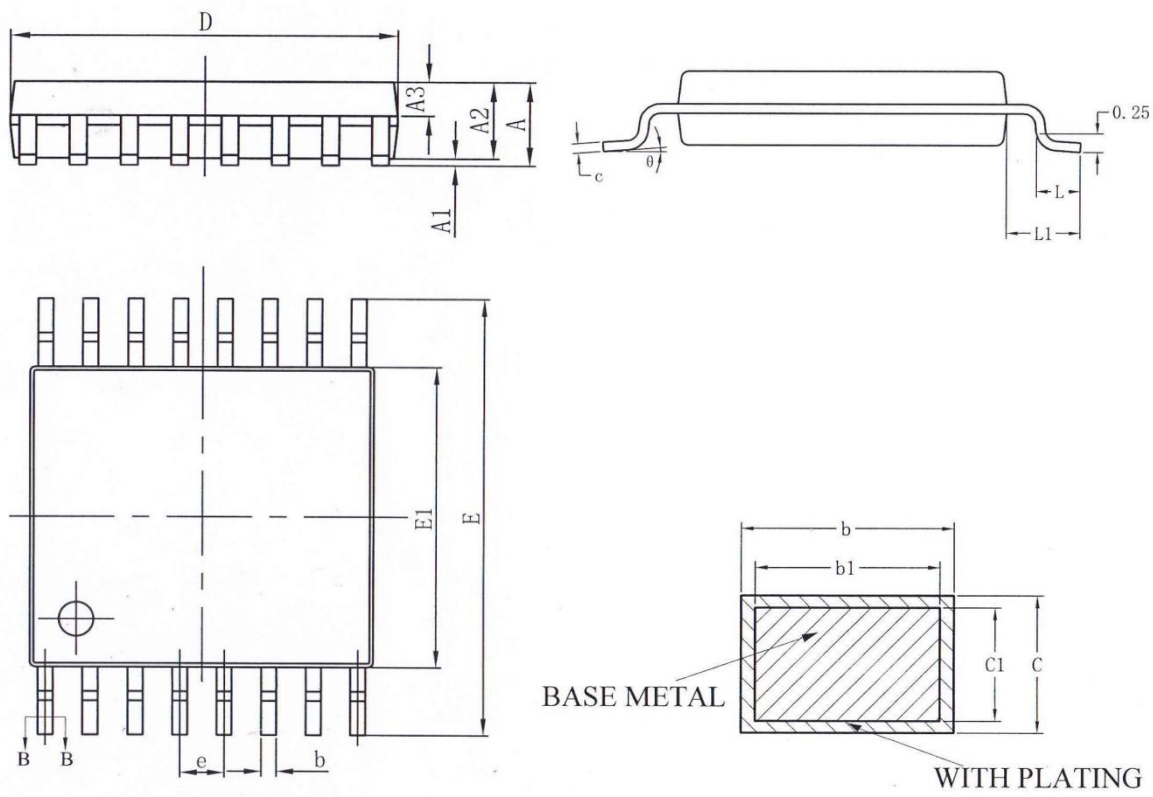


Figure8.LVDS Driver

PACKAGE DIMENSIONS(TSSOP-16)



SYMBOL	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Reflow profile

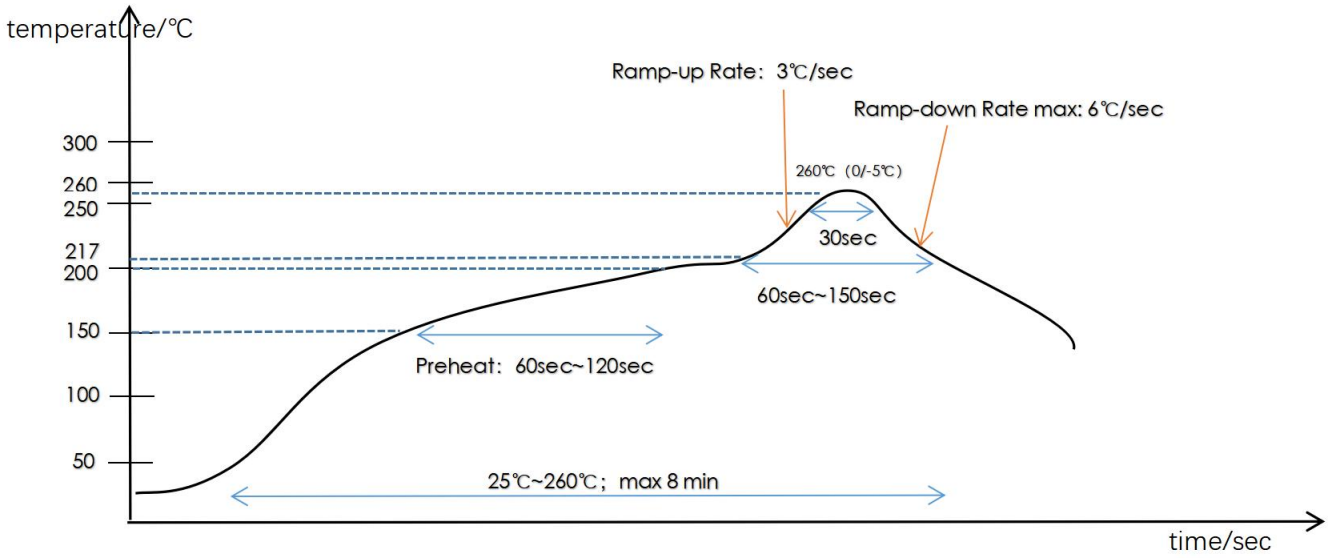


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.04.13	First Draft.	1.0
2023.05.11	Update Timing Diagrams.	1.5