Description

The US6D101C is a PCIe compliant clock generator. The device has 1 differential outputs. All clocks generated are derived from a single external 25-MHz crystal.

Recommended Applications

1 output synthesizer for PCIe Gen1/2/3/4/5 and Ethernet

Output Features

1 Non-spread 0.7V current mode differential HCSL output pairs.

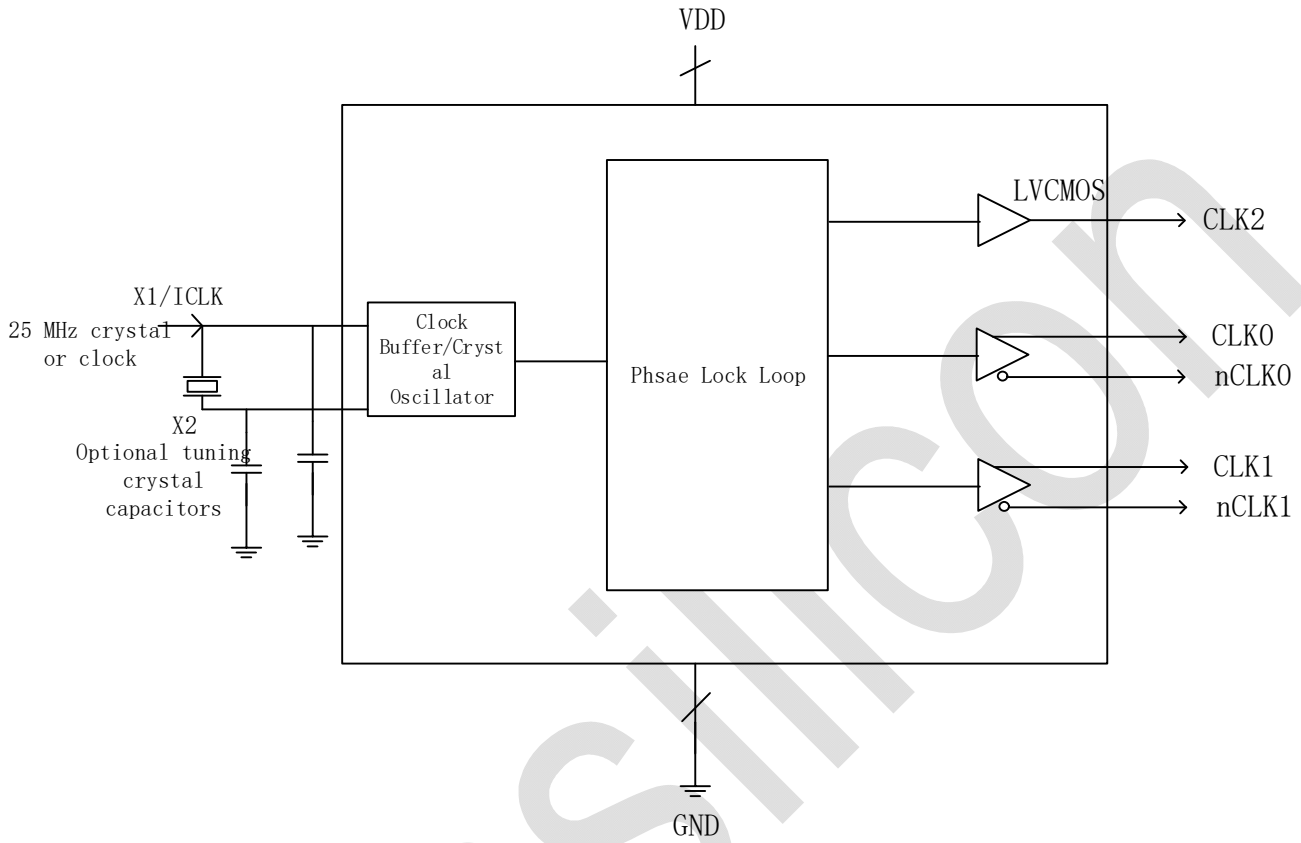
Features

- 16-pin QFN 3mmX3mm packages; small board footprint
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Supply voltage of 3.3V±10%
- Output-to-output skew <50 ps
- PCIe Gen2 phase jitter <3.0ps RMS
- The UltraClock® trademark used in connection with this product”
- Low phase noise:
  12kHz to 20MHz@100MHz : 158 fs RMS
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.7V current mode differential pair
- Industrial Temperature Range: -40°C to 85°C

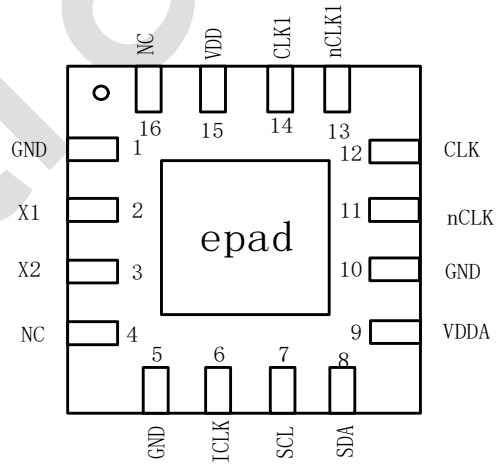
US6D101C and subtype table

Model	Output mode	Output Frequency(MHz)
US6D101C	HCSL(default)、LVPECL、LVDS、LVCMOS	52(default)、100、125...
US6D101C-D4	LVDS	CLK0/1: 125; CLK4: OFF
US6D101C-H3	HCSL	CLK0/1: 100; CLK4: OFF
US6D101C-XC3	LVCMOS	CLK0/1: OFF;CLK4: 100
US6D101C-C9	LVCMOS	CLK0/1: OFF;CLK4: 50

Block Diagram



Pin Assignment for QFN-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Pin Description
1	GND	Power	Connect to ground.
2	X1	Input	Crystal input. Connect to a 25 MHz crystal clock.
3	X2	Output	Crystal connection. Leave unconnected for clock input.
4	NC	–	No connect.
5	GND	Power	Connect to ground.
6	ICLK	Output	LVCMOS Output.
7	SCL	-	Serial Clock Input.
8	SDA	-	Serial Data Input/Output.
9	VDDA	Power	Connect to voltage supply +3.3 V for output driver and analog circuits
10	GND	Power	Connect to ground.
11	nCLK	Output	Complementary clock output.
12	CLK	Output	True clock output .
13	nCLK1	Output	Complementary clock output1.
14	CLK1	Output	True clock output1 .
15	VDD	Power	Connect to voltage supply +3.3 V for crystal oscillator and digital circuit.
16	NC	–	No connect.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 uF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the US6D101C to meet PCI Express specifications.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}, V_{DDOX}[1]	4.6V
V_{IN}	-0.5V to V_{DDOX}[1] + 0.5V
T_J :Junction Temperature	150°C
T_{STG} :Storage Temperature	-65°C to 150°C

NOTE 1. V_{DDOX} denotes V_{DDOA}, V_{DDOB} and VDDOC.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
V_{DDOX}[1]	Power supply for Bank QA or QB or REFOUT	3.3-5%	3.3	3.3+5%	V

Electrostatic level

		MAX	UNIT
V(ESD)	HBM模式, ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	MM模式, JEDEC Std. JESD22-A115-C	±250	
	CDM模式, ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up level

		MAX	UNIT
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Electrical Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply current	IDD			108.9		mA
Clock Input						
Input Frequency	F_{IN}			25		MHz
HCSL Clocks						
FOUT	Output Frequency		—	100	—	MHz
V_{OH}	Output High Voltage	VDD = 3.3V	660	800	850	mV
V_{OL}	Output Low Voltage		-150	0	27	mV
V_{OX}	Crossing Point Voltage	Absolute	250	350	550	mV
V_{CN}	Crossing Point Voltage	Variation over all edges			140	mV
FACC	Frequency Accuracy	All output clocks	—	—	100	ppm
TR/TF	Slew Rate	Measured differentially from ±150 mV		1.3	3.0	V/ns
$t_{jphPCIeG5-CC}$	PCIe Phase Jitter Common Clocked Architecture	PCIe Gen5 (32.0 GT/s)	—	70	90	fs
Jitter	Phase Jitter	12kHz to 20MHz@100MHz		158	300	fs
Skew	Output Skew	3.3V,HCSL@156.25MHz		33	40	ps
T_{OR}	Rise Time	From 20% to 80%		460	750	ps
T_{OF}	Fall Time	From 80% to 20%		460	750	ps
Duty Cycle	Duty Cycle		45		55	%

Applications Information

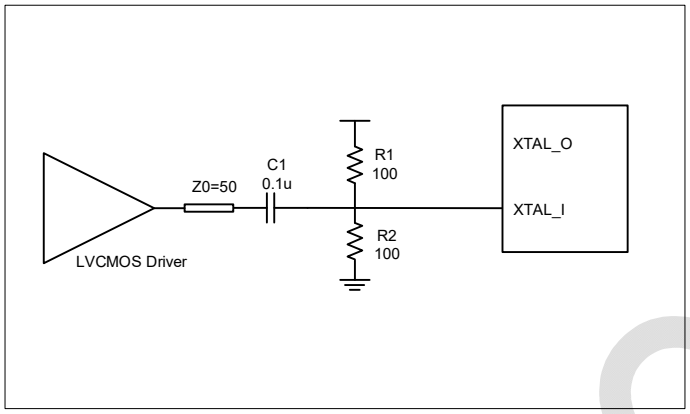
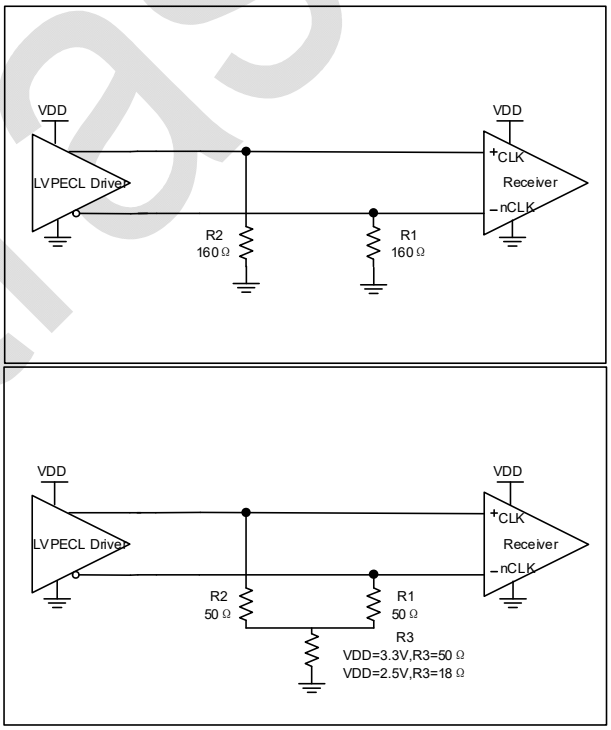
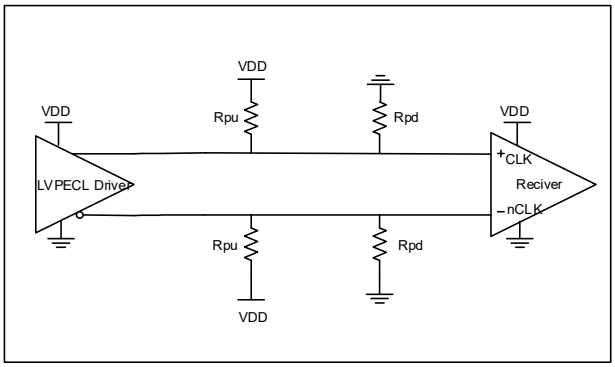


Figure1.Single-termination method

Output connection circuit

The clock topology shown below is a typical termination for LVPECL outputs. The two different terminations mentioned are recommended only as guidelines.The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ohm transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure2.LVPECL Driver

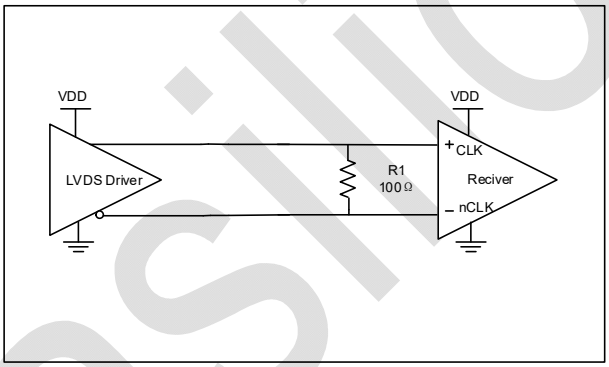


Figure3.LVDS Driver

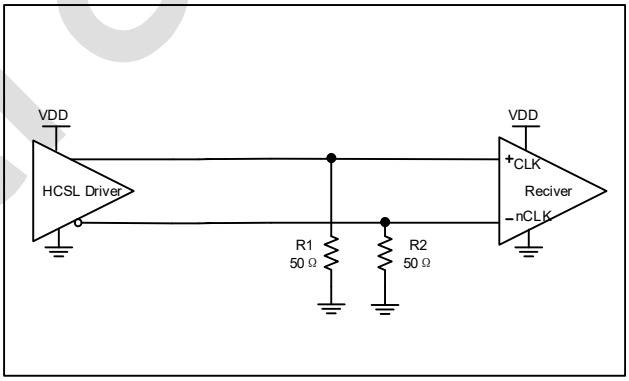
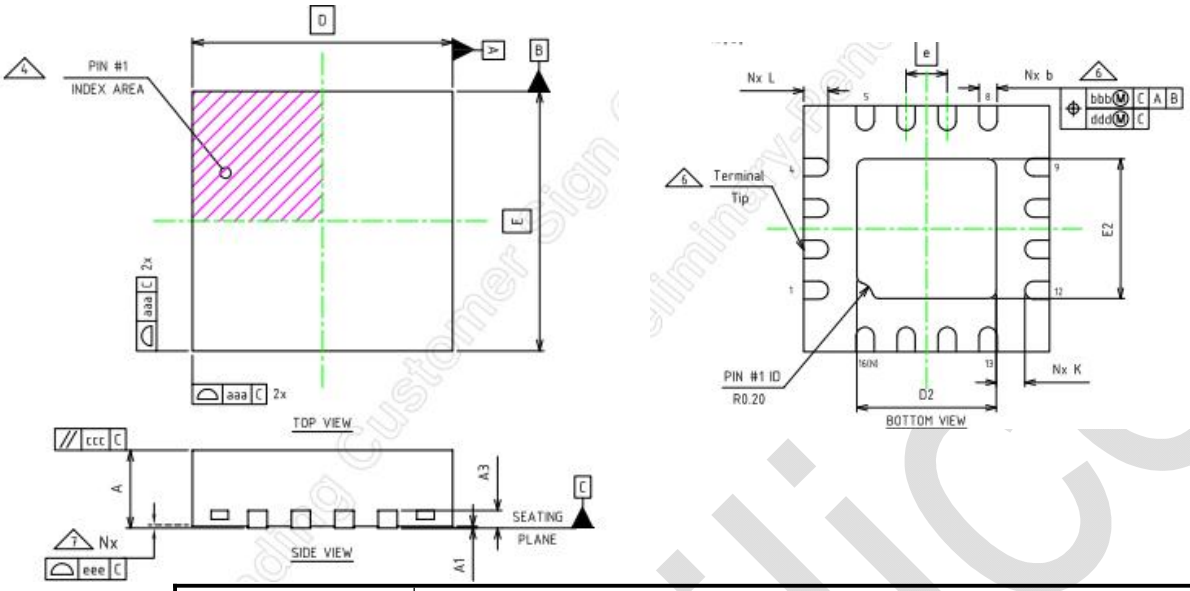


Figure4.HCSL Driver

Package Outlines



符号	单位：mm		
	最小值	典型值	最大值
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D2	1.60	1.70	1.80
E2	1.60	1.70	1.80
K	0.20	---	---
L	0.20	0.30	0.40
e		0.50 BSC	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Reflow profile

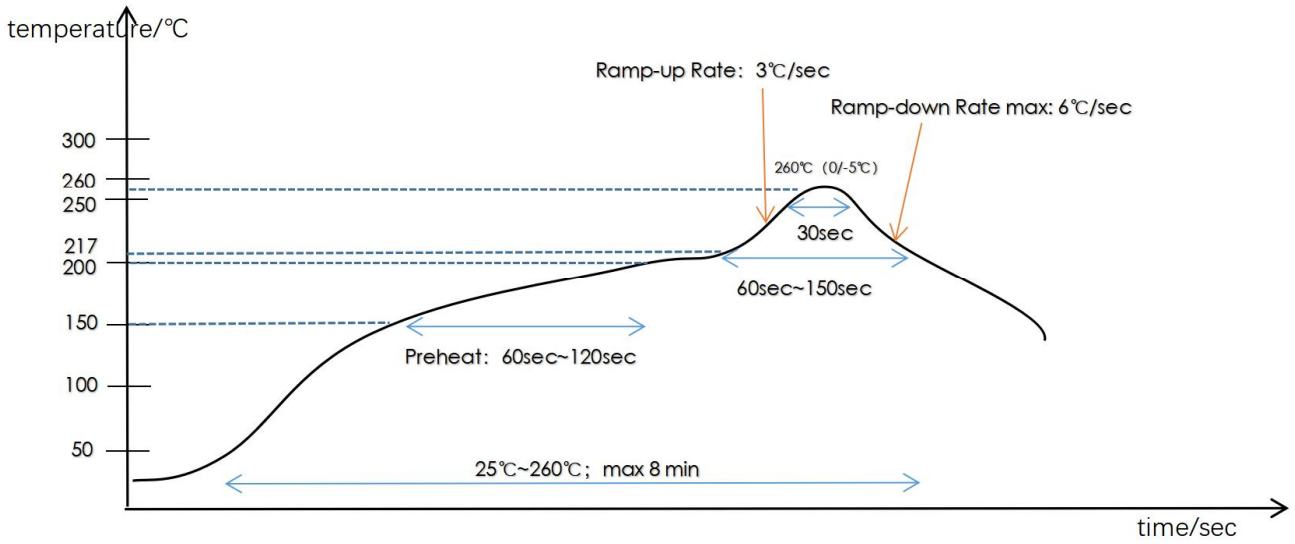


Figure5: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.1.30	First Draft.	1.0
2023.3.29	Add current characteristics	1.5
2024.9.25	Add the submodel table.	2.0
2026.1.23	Add product trademark.	2.5
2026.6.9	Modify the submodel table.	3.0